Intel® 64M20C Client Compute NAND Flash Memory

PF29F64G08LCMFS, PF29F16B08MCMFS, PF29F32B08NCMFS

Advance Datasheet

Product Features

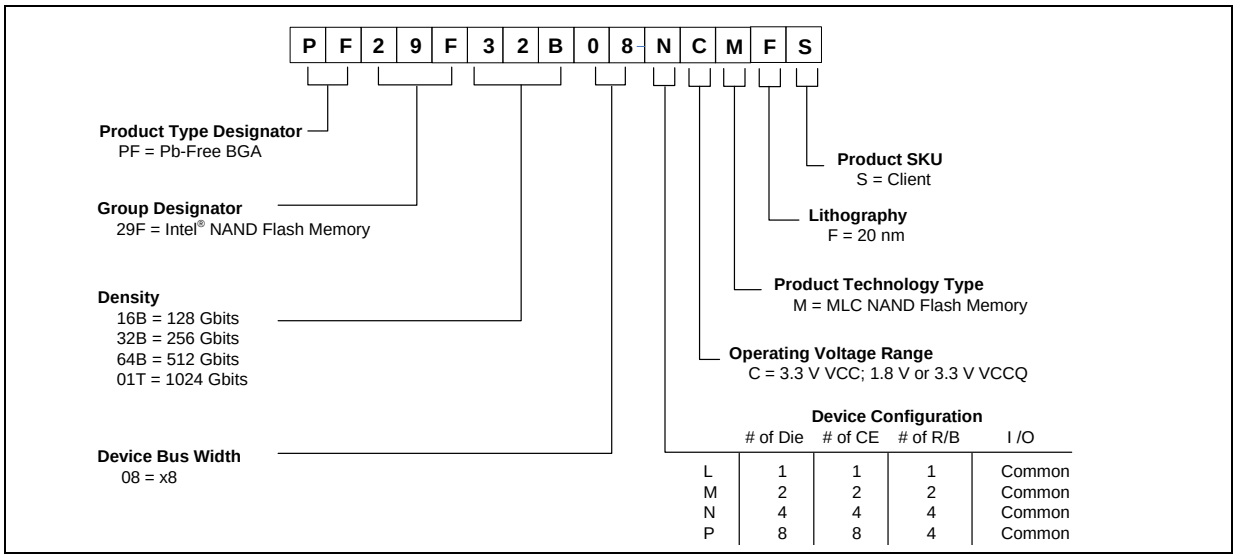
- Open NAND Flash Interface (ONFI) 3.0-compliant
- Multi-level cell (MLC) technology
- Organization
  - Page size: 17,600 bytes (16,384 + 1216)
  - Block size: 512 pages, (8,192K + 608K bytes)
  - Plane size: 2 planes x 512 blocks
- Device size:
  - 64 Gb: 1,024 blocks
  - 128Gb: 2,048 blocks
  - 256Gb: 4,096 blocks
- Synchronous I/O performance
  - Up to timing mode 6
  - Clock rate: 6ns
  - Read/write throughput per pin: 333 MT/s
- Asynchronous I/O performance
  - Up to asynchronous timing mode 5
  - ^{t}RC/^{t}WC: 20ns (MIN)
  - Read/write throughput per pin: 50 MT/s
- Array performance
  - Read page: 65us (TYP), 110us (MAX)
  - Program page: 1,250us (TYP)
  - Erase block: 5ms (TYP)
- Operating Voltage Range
  - VCC: 2.7–3.6V
  - VCCQ: 1.7–1.95V or 2.7–3.6V (Async only)
- Command set: ONFI NAND Flash Protocol
- Advanced command set:
  - PAGE CACHE PROGRAM
  - READ CACHE (RANDOM, SEQUENTIAL, END)
  - READ UNIQUE ID
  - COPYBACK
  - Multi-LUN operations
  - Multi-plane commands
  - Read unique ID
- Copyback operations supported within the plane that the data was read
- First block (block address 00h) is valid when shipped from factory.
- RESET (FFh) required as first command after power-on
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Data strobe (DQS) signals provide a hardware method for synchronizing data DQ in the synchronous interface
- On-die Termination (ODT)
- Operating temperature: 0°C to +70°C
- Package: 132-ball BGA

Density	Package	# of Die		# of CE# and R/B#	Bus I/O Configuration	Device ID
64Gb	BGA	SDP	1	1	Single x8	89h, 64h, 64h, 3Ch, A1h, 00h, 00h, 00h
128Gb	BGA	DDP	2	2	Dual x8	89h, 64h, 64h, 3Ch, A1h, 00h, 00h, 00h
256Gb	BGA	QDP	4	4	Dual x8	89h, 64h, 64h, 3Ch, A1h, 00h, 00h, 00h

Ordering Information

Intel® NAND Flash Memory devices are available in different configurations and densities.

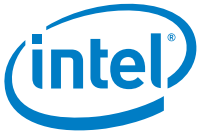
Decoder



Intel® NAND Flash Memory Ordering Information

Device Name	MM #	Device Nomenclature
PF29F64G08LCMFS	926372	64 Gb 1x8 SDP, 1 CE, 1 R/B, 3.3 V 132 BGA (Engineering Sample)
PF29F16B08MCMFS	926373	128 Gb 2x8 DDP, 2 CE, 2 R/B, 3.3 V 132 BGA (Engineering Sample)
PF29F32B08NCMFS	926374	256 Gb 2x8 QDP, 4 CE, 4 R/B, 3.3 V 132 BGA (Engineering Sample)

Contents



1.0 Overview

NAND flash technology provides a cost-effective solution for applications requiring high-density solid-state storage. The Intel® 64M20C device is available in three densities:

- 64 Gb
- 128 Gb
- 256 Gb

Intel® NAND Flash Memory devices include standard NAND flash features and new features designed to enhance system-level performance. For a summary of performance and reliability specifications, see "Product Features" on page 1. Details are available in subsequent sections in this document.

These NAND devices are ONFI 3.0-compliant and support an asynchronous interface only. The ONFI 3.0 specification can be found at www.onfi.org.

1.1 Architecture

Intel NAND Flash Memory devices offer an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (DQx) to transfer commands, addresses, and data.

Five control signals implement the asynchronous interface: CE#, CLE, ALE, WE# and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

Some versions of this Intel NAND Flash device additionally include a synchronous data interface for high-performance I/O operations. When the synchronous interface is active, WE# becomes CLK and RE# becomes W/R#. Data transfers include a bidirectional data strobe (DQS).

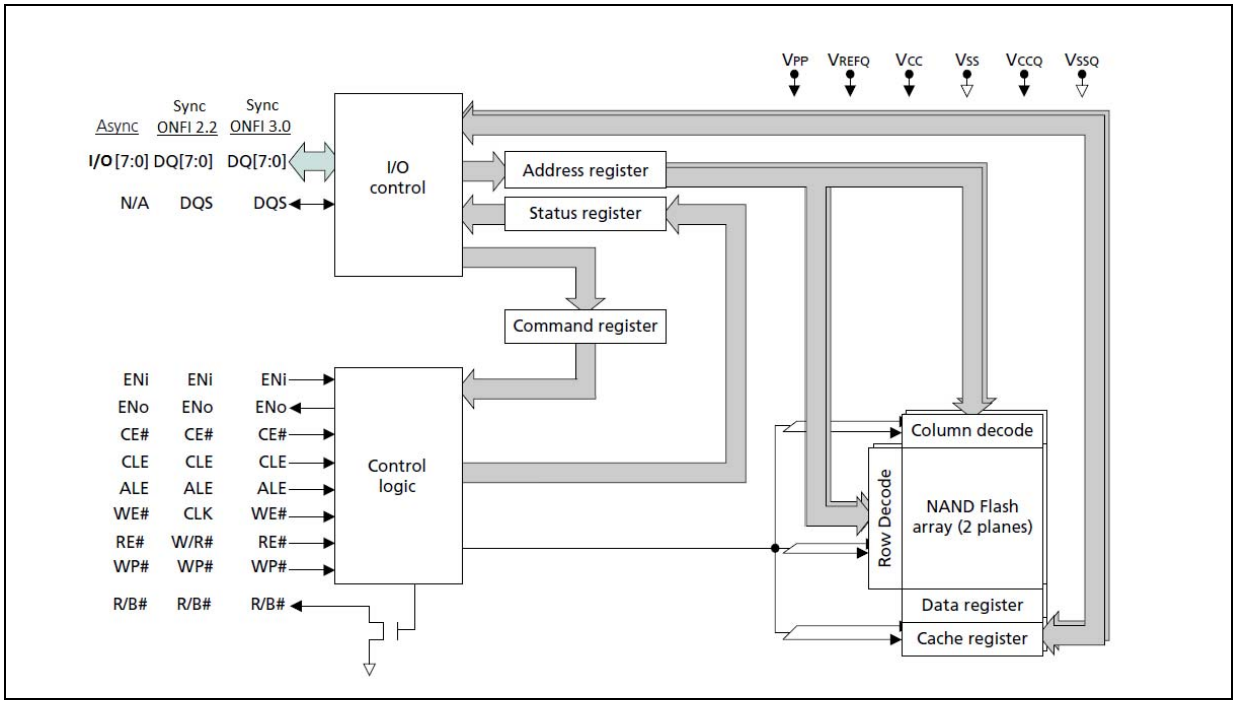
This hardware interface creates a low-pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND flash die. A NAND flash die is the minimum unit that can indepentently execute commands and report status. A NAND flash die in the ONFI specification is referred to as a logical unit (LUN). There is one LUN per CE#.

The contents of each page can be programmed in ^{t}PROG, and an entire block can be erased in ^{t}BERS.

1.2 Block Diagram

Figure 1. NAND Flash Memory Functional Block Diagram



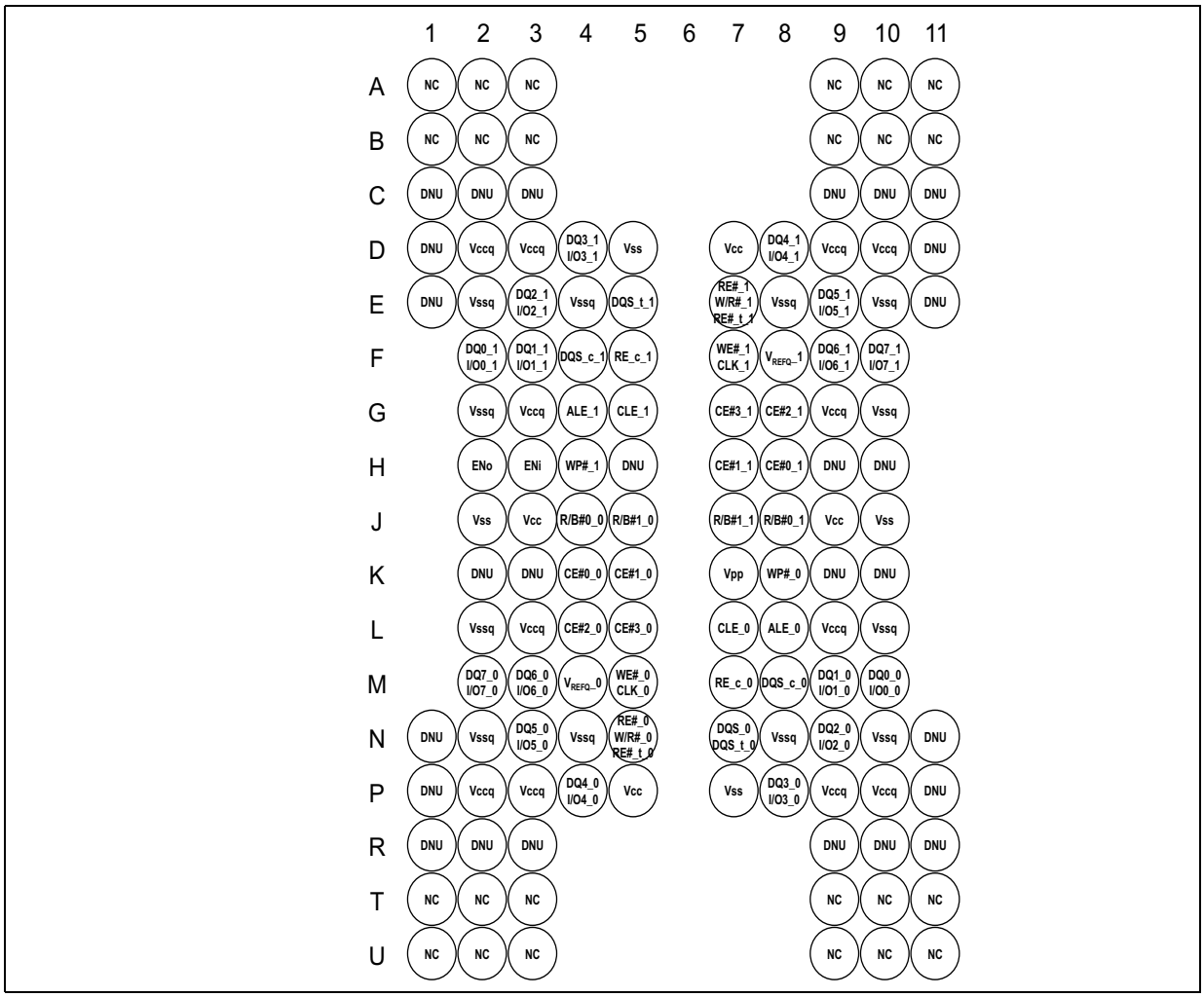
1.3 Addressing

NAND flash devices do not contain dedicated address pins. Addresses are loaded using a five-cycle sequence, as shown in Table 2, “Array Addressing for 64Gb LUN” on page 16. See Figure 8, “Memory Map 64 Gb” on page 14 for additional memory mapping and addressing details.

2.0 Packaging Information

2.1 Pin Assignments

Figure 2. 132-Ball BGA (Top View)



2.2 Signal Descriptions

Table 1. BGA Signal Descriptions

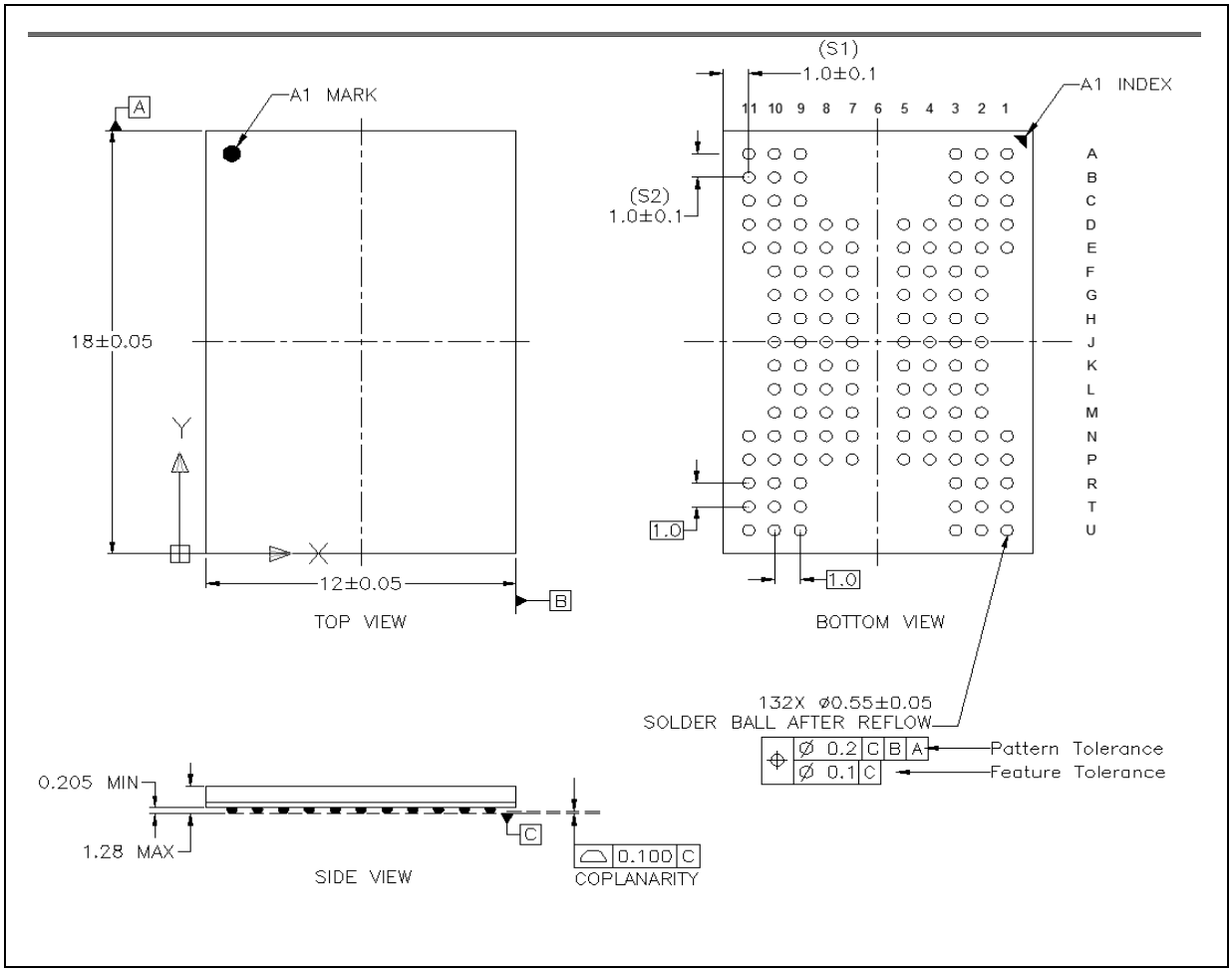
Asynchronous Symbol	Synchronous Symbol (ONFI 2.3)	Synchronous Symbol (ONFI 3.0)	Type	Pin Function
ALE_0, ALE_1	ALE_0, ALE_1	ALE_0, ALE_1	Input	**Address Latch Enable** During the time ALE is HIGH, address information is transferred from I/O[7:0] into the on-chip address register on the rising edge of WE#. When address information is not being loaded, ALE should be driven LOW.
CE#[0:3]_0, CE#[0:3]_1	CE#[0:3]_0, CE#[0:3]_1	CE#[0:3]_0, CE#[0:3]_1	Input	**Chip Enable** Gates transfers between the host system and the NAND flash device. Once the device starts a PROGRAM or ERASE operation, CE# can be de-asserted. Each CE# controls a single LUN.
CLE_0, CLE_1	CLE_0, CLE_1	CLE_0, CLE_1	Input	**Command Latch Enable** When CLE is HIGH, information is transferred from I/O[7:0] to the on-chip command register on the rising edge of WE#. When command information is not being loaded, CLE should be driven LOW.
I/O[7:0]_0, I/O[7:0]_1	DQ[7:0]_0, DQ[7:0]_1	DQ[7:0]_0, DQ[7:0]_1	I/O	**Data Inputs/Outputs** The bidirectional I/Os transfer address, data, and command information.
—	DQS_0, DQS_1	DQS_t_0, DQS_c_1	I/O	**Data Strobe** Provides a synchronous reference for data input and output.
—	—	DQS_c_0, DQS_c_1	I/O	**Data Strobe** Provides a completmentary signal to the data strobe signal optionally used in the synchronous interface for synchronous reference for data input and output.
ENi	ENi	ENi	Input	**Enumerate Input** Input to a NAND device (if first NAND device on the daisy chain has as NC) from ENo of a previous NAND device to support CE# pin reduction functionality.
ENo	ENo	ENo	Output	**Enumerate Output** Output from a NAND device to the ENi of the next NAND device in the daisy chain to support CE# pin reduction functionality.
RE#_0, RE#_1	W/R#_0, W/R#_1	RE_t_0, RE_t_1	Input	**Read Enable and Write/Read** RE# transfers serial data from the NAND Flash to the host system when the asynchronous interface is active. When the synchronous interface is active, W/R# controls the direction of DQx and DQS.
-	-	RE_c_0, RE_c_1	Input	**Read enable complement** Provides a complimentary signal to the read enable signal optionally used in the synchronous interface for synchronous reference for data output.
WE#_0, WE#_1	CLK_0, CLK_1	WE#_0, WE#_1	Input	**Write Enable and Clock** WE# transfers commands and addresses addresses when the asynchronous and synchronous interfaces are active, and serial data from the host system to the NAND Flash when the asynchronous interface is active. When the synchronous interface is active, CLK latches command and address cycles.
WP#_0, WP#_1	WP#_0, WP#_1	WP#_0, WP#_1	Input	**Write Protect** Pin protects against inadvertent PROGRAM and ERASE operations. All PROGRAM and ERASE operations are disabled when WP# is LOW.

Table 1. BGA Signal Descriptions

Asynchronous Symbol	Synchronous Symbol (ONFI 2.3)	Synchronous Symbol (ONFI 3.0)	Type	Pin Function
R/B#[0:1]_0, R/B#[0:1]_1	R/B#[0:1]_0, R/B#[0:1]_1	R/B#[0:1]_0, R/B#[0:1]_1	Output	**Ready/Busy** An *open-drain*, active-LOW output that uses an external pull-up resistor. The pin is used to indicate when the chip is processing a PROGRAM or ERASE operation. It is also used during a READ operation to indicate when data is being transferred from the array into the serial data register. Once these operations have completed, R/B# returns to the high-impedance state.
V_{CC}	V_{CC}	V_{CC}	Supply	**Core power supply**
V_{CCQ}	V_{CCQ}	V_{CCQ}	Supply	**I/O power supply**
V_{PP}	V_{PP}	V_{PP}	Supply	Optional external high-voltage power supply to the device. This high voltage power supply may be used to enhance operations (for example, improve power efficiency).
V_{SS}	V_{SS}	V_{SS}	Supply	**Ground connection**
V_{SSQ}	V_{SSQ}	V_{SSQ}	Supply	**Ground connection**
-	-	V_{REFQ}_0, V_{REFQ}_1	Supply	Reference voltage used with synchronous interface.
NC	NC	NC	–	**No Connect** NC pins are not internally connected. These pins can be driven or left unconnected.
DNU	DNU	DNU	–	**Do Not Use** DNU pins must be left disconnected.

2.3 Mechanical Drawing

Figure 3. 132-Ball BGA Package Dimensions (1.28mm Z-height)



Note: All dimensions in millimeters; MIN, MAX, or TYP, as noted.

3.0 Configurations

Figure 4. SDP BGA Configuration

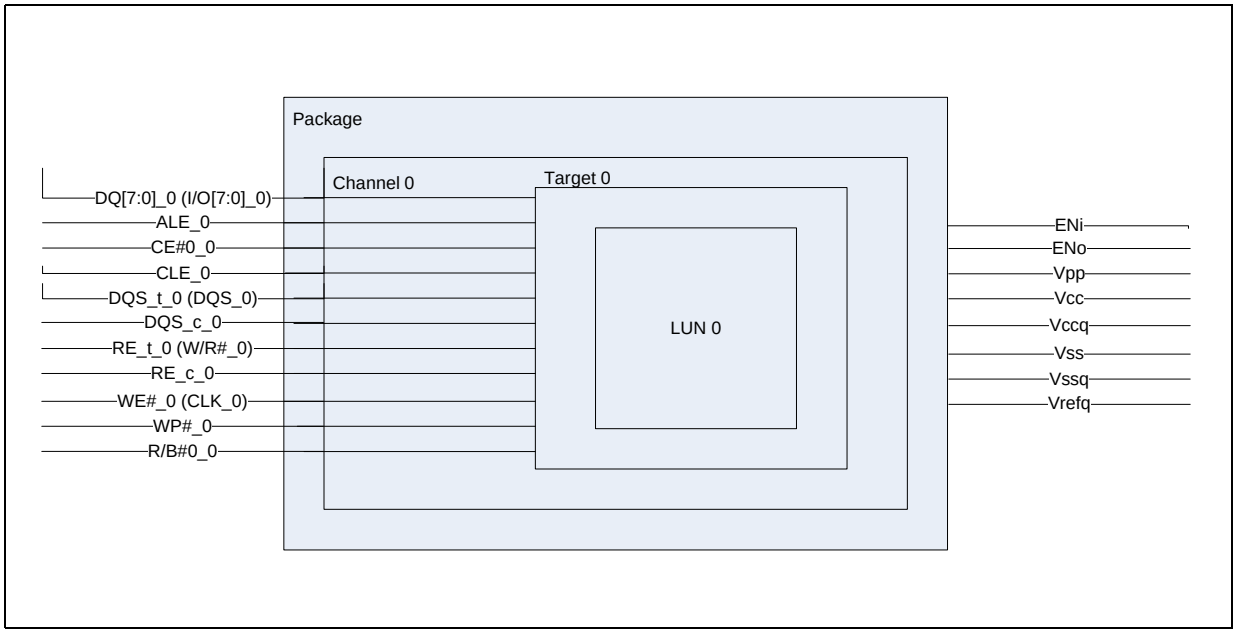


Figure 5. DDP BGA Configuration

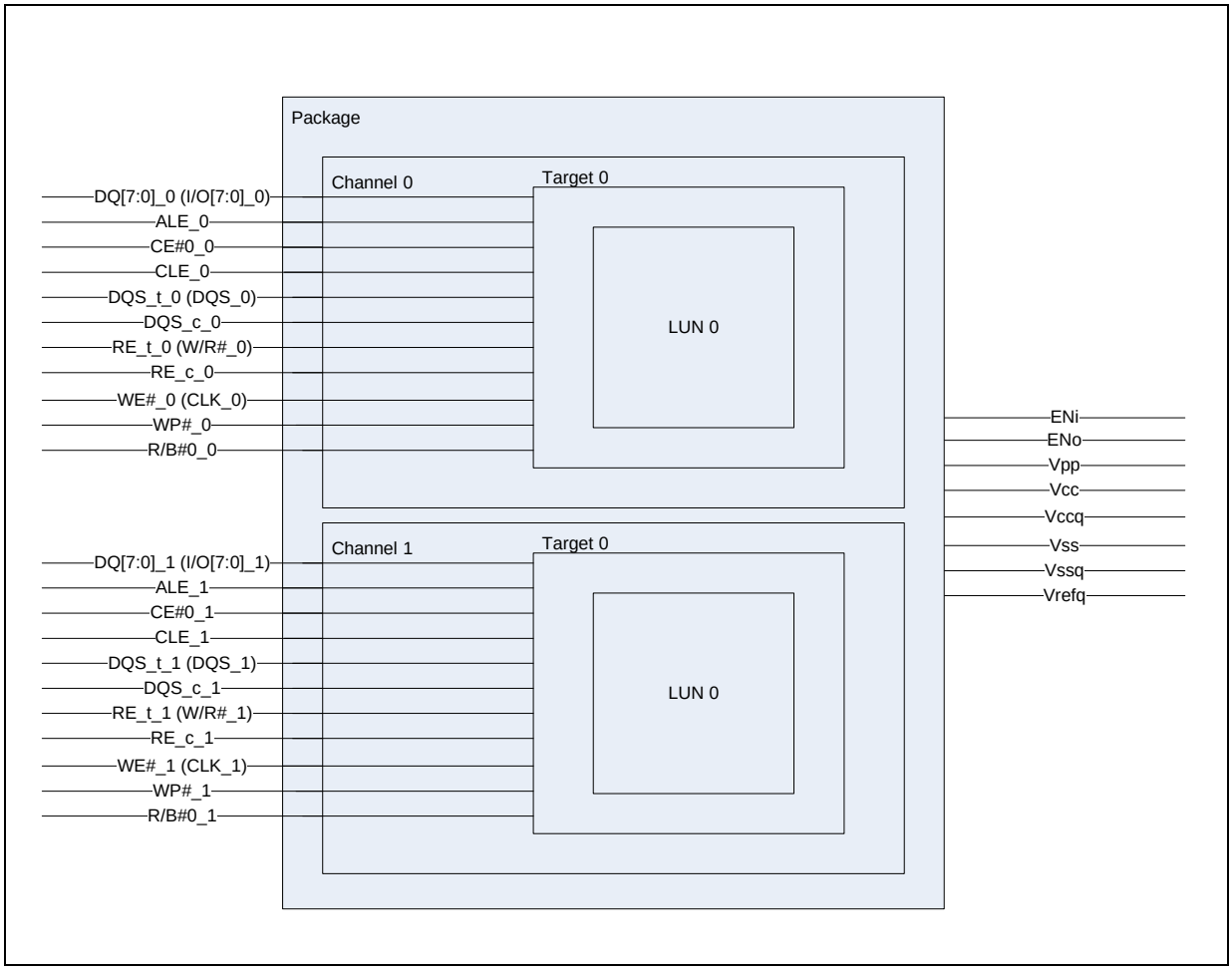
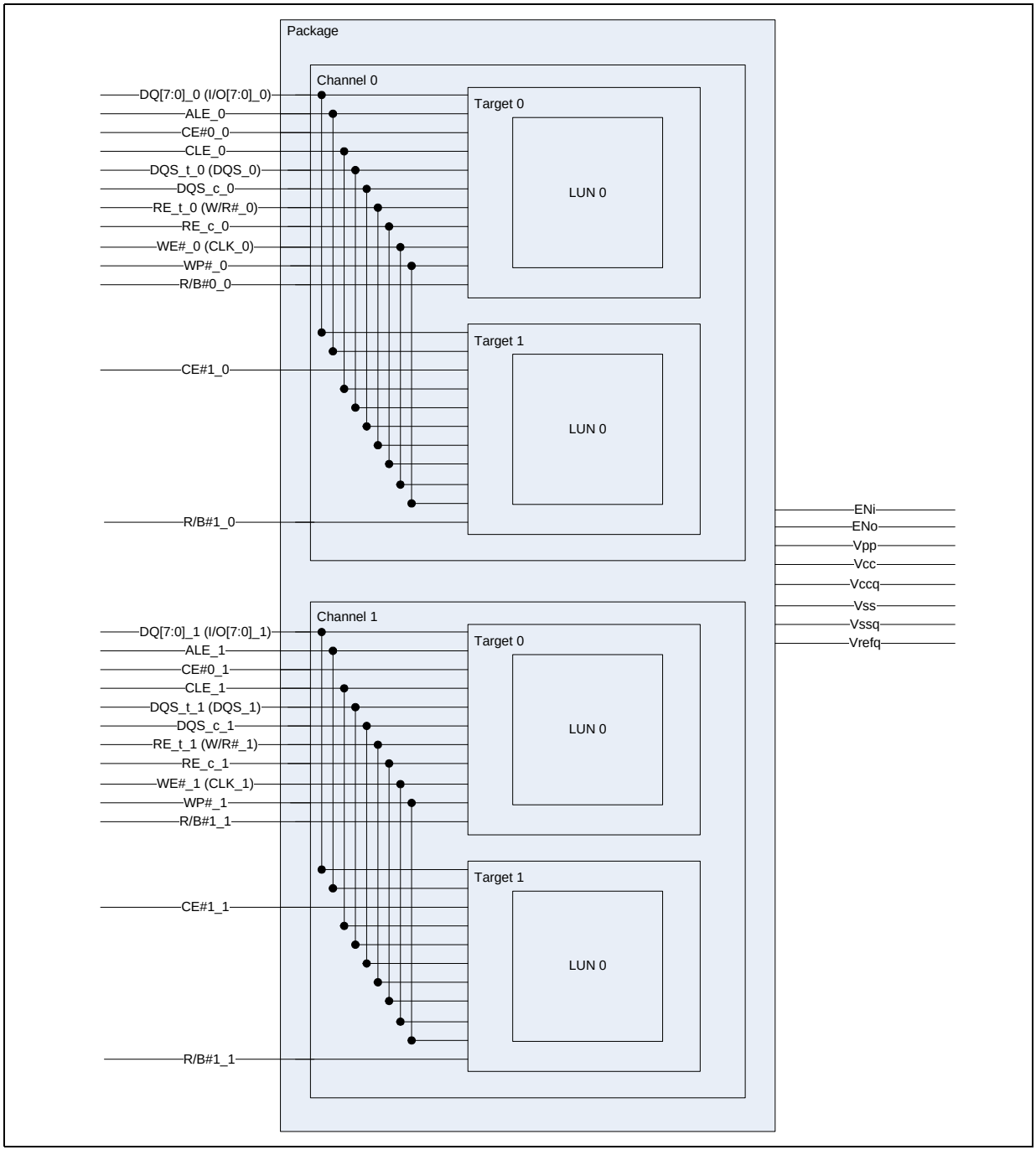


Figure 6. QDP BGA Configuration



4.0 Array Organization

Figure 7. Array Organization per Logical Unit (LUN)

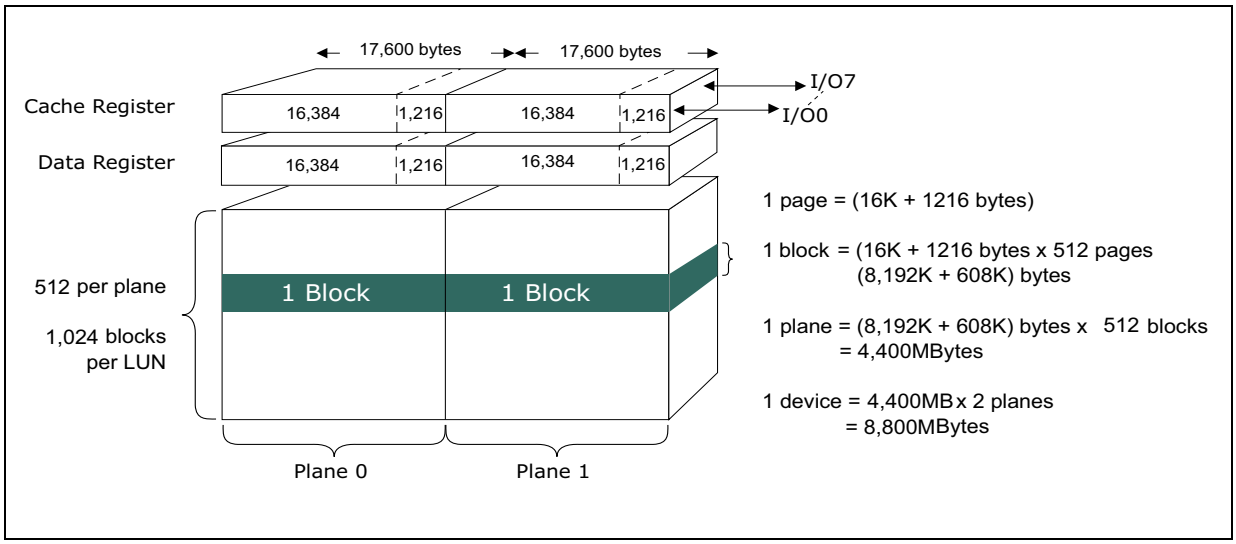


Table 2. Array Addressing for 64Gb LUN

Cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	CA14[3]	CA13[2]	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9[3]	PA8
Fifth	LOW	LOW	LA1[3]	LA0[5]	BA19	BA18	BA17	BA16

Notes:

1. The page address, block address, and LUN address are collectively called the *row address*.
   CAx = column address
   PAx = page address
   BAx = block address
2. Column addresses 17,600 (44C0h) through 32,767 (7FFFh) are invalid or *out of bounds;* they do not exist and cannot be addressed.
3. Plane select bit (BA[8])
   Plane 0 = BA[9] = 0
   Plane 1 = BA[9] = 1

5.0 Bus Operation — Asynchronous Interface

The asynchronous interface is active when the NAND Flash device powers on. The I/O bus, I/O[7:0], is multiplexed sharing data I/O, addresses, and commands. The DQS signal, if present, is tri-stated when the asynchronous interface is active.

Asynchronous interface bus modes are summarized below.

Table 3. Asynchronous Interface Mode Selection

Mode	CE#	CLE	ALE	WE#	RE#	I/O[7:0]	WP#	Notes
Standby	H	X	X	X	X	X	0 V/Vccq[2]	2
Bus Idle	L	X	X	H	H	X	X	
Command Input	L	H	L	↑	H	input	H	
Address Input	L	L	H	↑	H	input	H	
Data Input	L	L	L	↑	H	input	H	
Data Output	L	L	L	H	↓	output	X	
Write Protect	X	X	X	X	X	X	L	

Notes:
1. WP# should be biased to CMOS HIGH or LOW for standby.
2. Mode selection settings for this table:
   H = Logic level HIGH
   L = Logic level LOW
   X = VIH or VIL

5.1 Asynchronous Enable / Standby

A chip enable (CE#) signal is used to enable or disable a target. When CE# is driven LOW, all of the signals for that target are enabled. With CE# LOW, the target can accept commands, addresses, and data I/O. There may be more than one target in a NAND Flash package. Each target is controlled by its own chip enable; the first target (Target 0) is controlled by CE#; the second target (if present) is controlled by CE2#, etc.

A target is disabled when CE# is driven HIGH, even when the target is busy. When disabled, all of the target's signals are disabled except CE#, WP#, and R/B#. This functionality is also known as CE# "Don't Care". While the target is disabled, other devices can utilize the disabled NAND signals that are shared with the NAND Flash.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations. Standby helps reduce power consumption.

5.2 Asynchronous Bus Idle

A target's bus is idle when:

- CE# is LOW,
- WE# is HIGH,
- RE# is HIGH

While the bus is idle, all signals are enabled except DQS, which is not used when the asynchronous interface is active. No commands, addresses or data are latched into the target; no data is output.

5.3 Control Signals

CE#, WE#, RE#, CLE, ALE and WP# control flash device READ and WRITE operations.

CE# enables the corresponding LUN. When CE# is LOW and the LUN is not in the busy state, the flash memory accepts command, address, and data information.

When the LUN is not performing an operation, the CE# pin is typically driven HIGH and the LUN enters standby mode. The memory enters standby if CE# goes HIGH while data is being transferred and the LUN is not busy. This helps reduce power consumption.

The CE# *Don't Care* operation allows the NAND flash to reside on the same memory bus as other flash or SRAM devices. Other LUNs on the memory bus can then be accessed while the NAND flash is busy with internal operations. This capability is important for designs that require multiple NAND flash LUNs on the same bus. One LUN can be programmed while another is being read. See Figure 89 on page 143 and Figure 95 on page 148 for examples of CE# *Don't Care* operations.

A HIGH CLE signal indicates that a command cycle is occuring. A HIGH ALE signal signifies that an address input cycle is occurring.

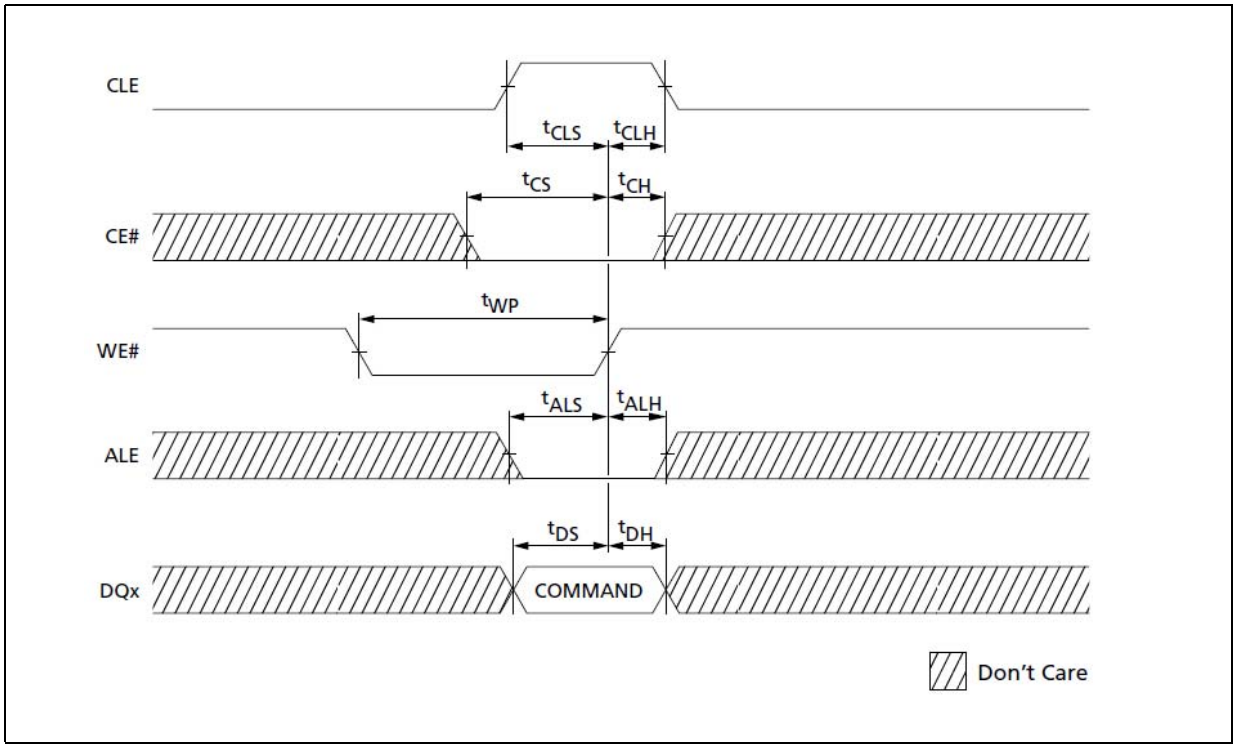
5.4 Asynchronous Commands

An asynchronoush command is written from I/O[7:0] to the command register on the rising edge of WE# when:

- CE# is LOW,
- ALE is LOW,
- CLE is HIGH,
- RE# is HIGH

Commands are typically ignored by LUNs that are busy; however, the device accepts the READ STATUS (70h), READ STATUS ENHANCED (78h), and RESET (FFh) commands when busy.

Figure 8. Asynchronous Command Latch



5.5 Address Input

An asynchronous address is written from I/O[7:0] to the address register on the rising edge of WE# when:

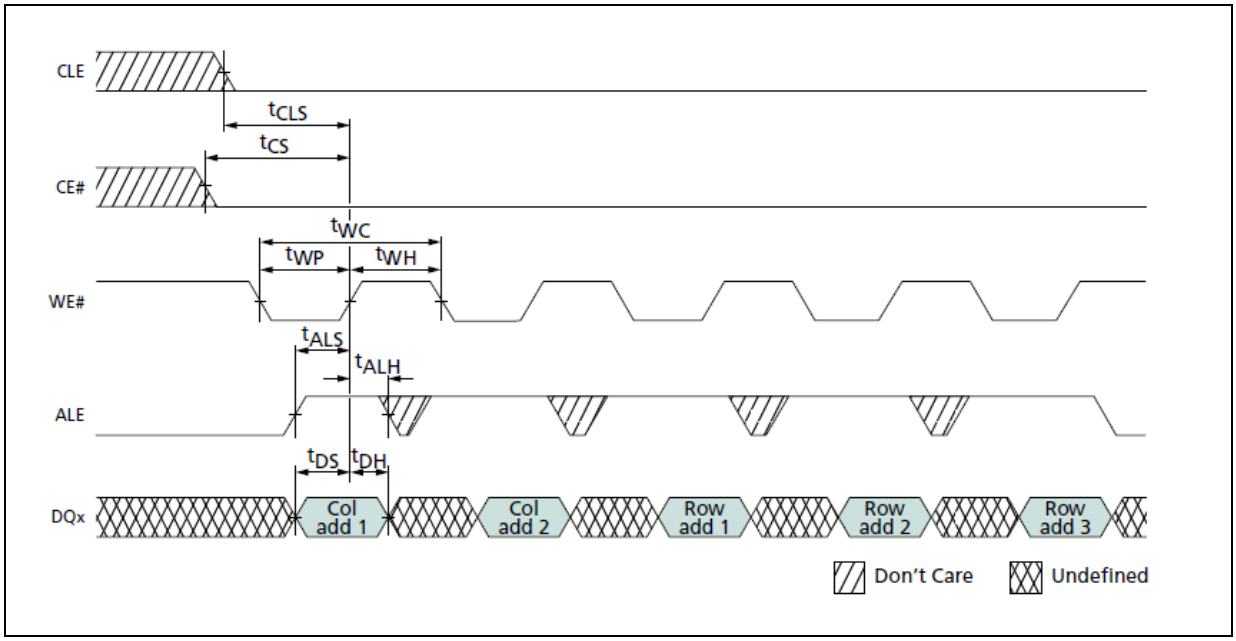
- CE# is LOW,
- CLE is LOW,
- ALE is HIGH,
- RE# is HIGH

Bits not part of the address space must be LOW. See Table 2, “Array Addressing for 64Gb LUN” on page 16.

The number of ADDRESS cycles required for each command varies. See Section 11.0, “Command Definitions” on page 63 to determine addressing requirements.

Addresses are typically ignored by busy LUNs; however, some addresses are accepted by busy LUNS, such as address cycles that follow the READ STATUS ENHANCED (78h) command.

Figure 9. Asynchronous Address Latch



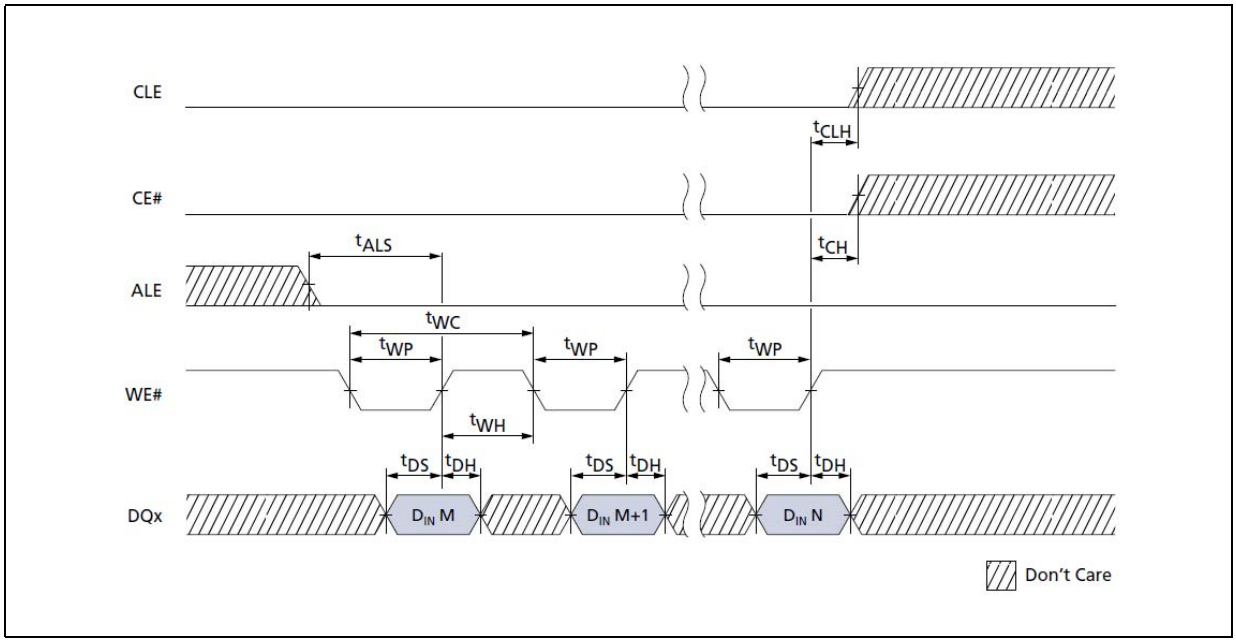
5.6 Asychronous Data Input

Data is written from I/O[7:0] to the data register of the selected die (LUN) on the rising edge of WE# when:

- CE# is LOW,
- CLE is LOW,
- ALE is LOW,
- RE# is HIGH

Busy (RDY = 0) or nonselected LUNs ignore data input unless the LUN is busy with a PAGE CACHE PROGRAM (80h - 15h) command operation.

Figure 10. Asynchronous Data Input Cycles



5.7 Asynchronous Data Output

Data can be output from a die (LUN) if it is in a READY state. Data output is supported following a READ operation from the NAND Flash array. Data is output from the cache register of the selected die (LUN) to I/O[7:0] on the falling edge of RE# when:

- CE# is LOW
- ALE is LOW
- CLE is LOW
- WE# is HIGH

If the host controller is using a tRC of 30ns or greater, the host can latch the data on the rising edge of RE# (see Figure 11 for proper timing). If the host controller is using a tRC of less than 30ns, the host can latch the data on the next falling edge of RE# (see Figure 12 for extended data output (EDO) timing).

Using the READ STATUS ENHANCED (78h) command prevents data contention following an interleaved die (multi-LUN) operation. After issuing the READ STATUS ENHANCED (78h) command, to enable data output, issue the READ MODE (00h) command.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by first issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

Figure 11. Asynchronous Data Output Cycles

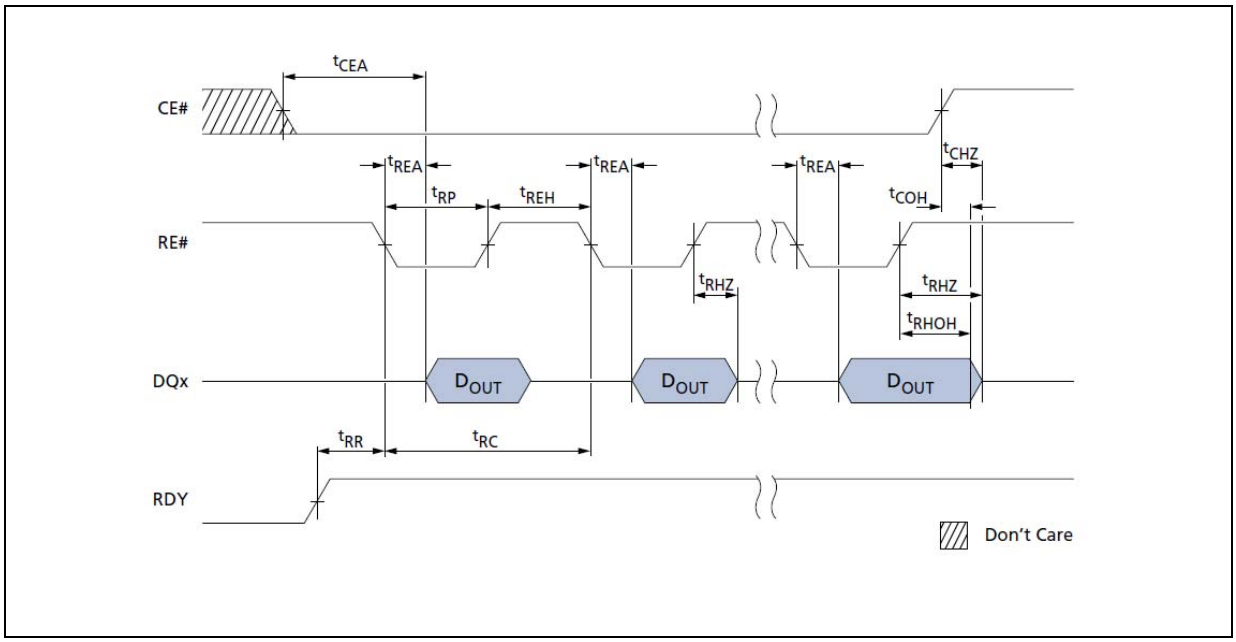
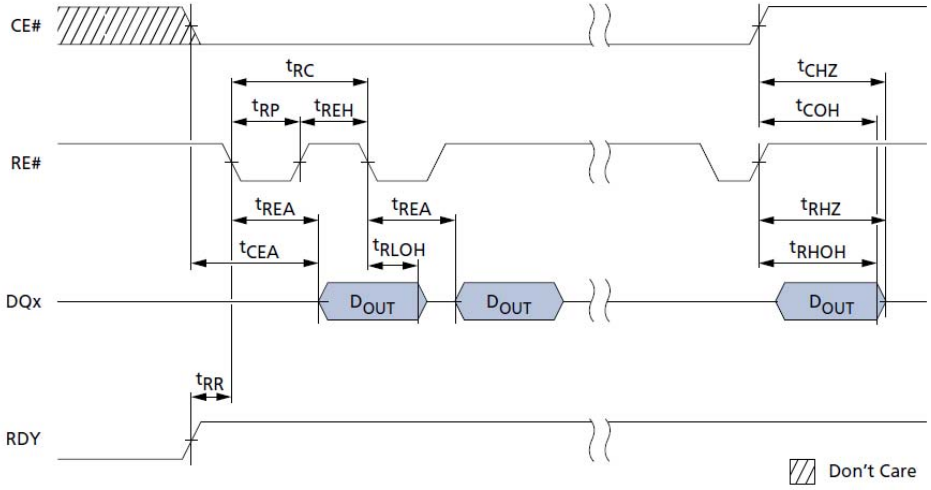


Figure 12. Asynchronous Data Output Cycles (EDO Mode)



5.8 Write Protect

The write protect# (WP#) signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled.

It is recommended that the host drive WP# LOW during power-on until Vcc and Vccq are stable to prevent inadvertent PROGRAM and ERASE operations "Power Cycle Requirements" on page 121 for additional details).

WP# must be transitioned only when the target is not busy and prior to beginning a command sequence. After a command sequence is complete and the target is ready, WP# can be transitioned. After WP# is transitioned, the host must wait tWW before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

5.9 Ready/Busy#

The ready/busy# (R/B#) signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its die (LUNs) are busy (RDY = 0). A target is ready when all of its die (LUNs) are ready (RDY = 1). Because each die (LUN) contains a status register, it is possible to determine the independent status of each die (LUN) by polling its status register instead of using the R/B# signal (see Section 15.0, “Status Operations” on page 82 for details regarding die (LUN) status).

This signal requires a pull-up resistor, Rp, for proper operation. R/B# is HIGH when the target is ready, and transitions LOW when the target is busy. The signal's open-drain driver enables multiple R/B# outputs to be OR-tied. Typically, R/B# is connected to an interrupt pin on the system controller (see Figure 13).

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. Between the 10-to 90-percent points on the R/B# waveform, the rise time is approximately two time constants (TC).

Figure 13. Time Constants

$$TC = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# pin and the total load capacitance. Approximate Rp values using a circuit load of 100pF are provided in Figure 20 on page 27.

Figure 16 on page 25 and Figure 18 on page 26 depict approximate Rp values using a circuit load of 100 pF.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and V_{CC}.

Figure 14. Minimum Rp

$$Rp\ (MIN) = \frac{V_{CCQ}\ (MAX) - V_{OL}\ (MAX)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

Where ΣI_L is the sum of the input currents of all devices tied to the R/B# pin.

Figure 15. Ready/Busy# Open Drain

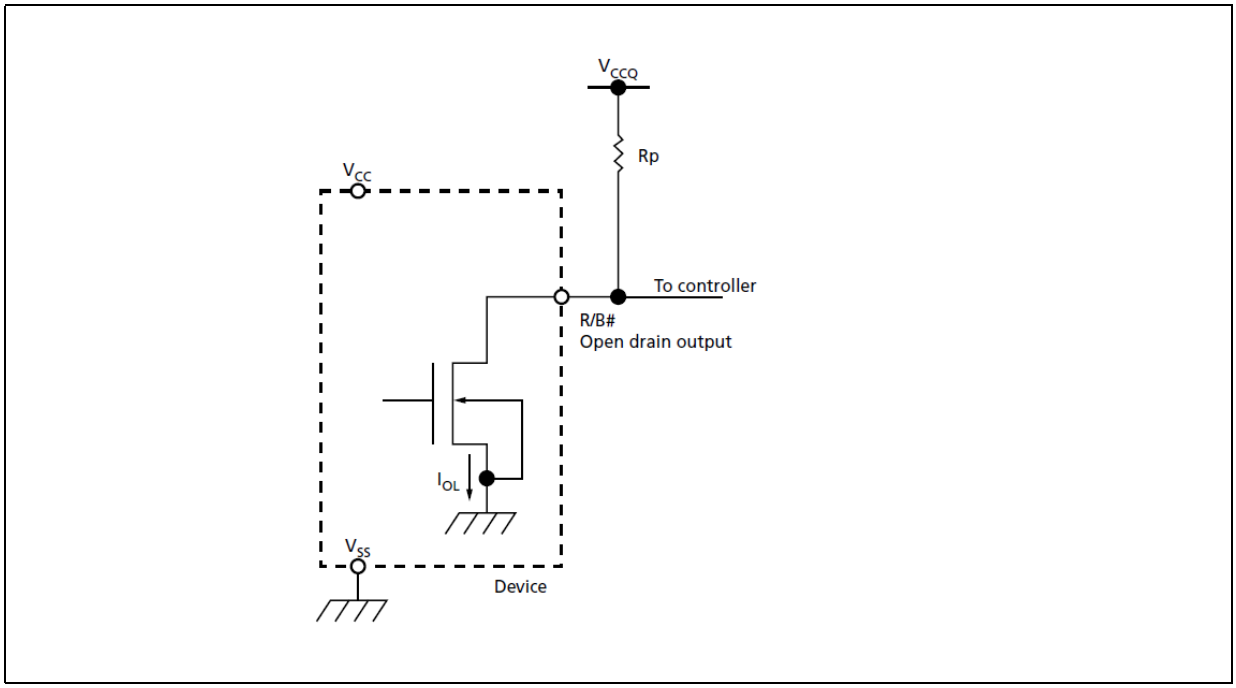
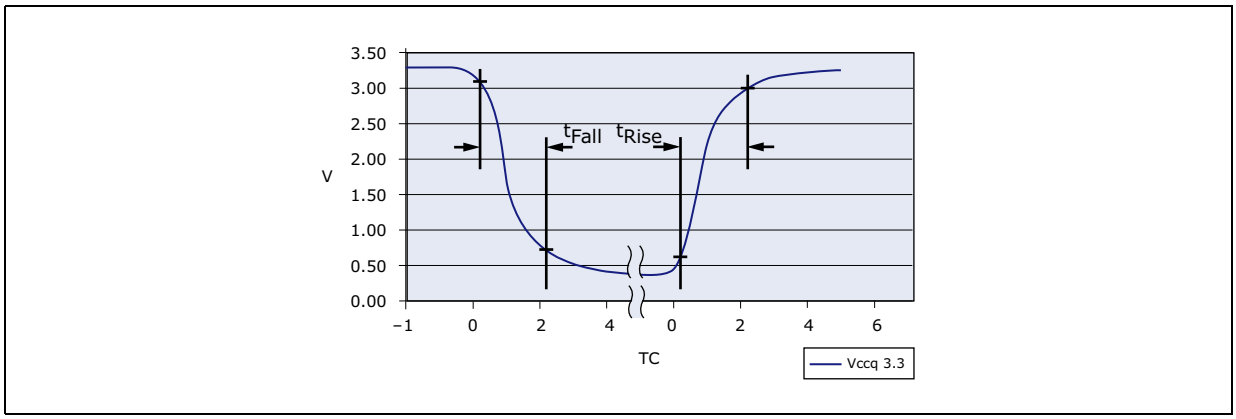
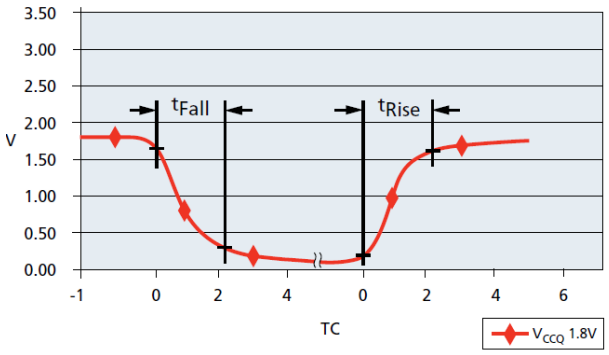


Figure 16. tFall and tRise (V_{CCQ} = 2.7-3.6V)



Notes:
1. tFall and tRise calculated at 10 percent–90 percent points.
2. tRise dependent on external capacitance and resistive loading, and output transistor impedance.
3. tRise primarily dependent on external pull-up resistor and external capacitive loading.
4. tFall ≈ 10 ns at Vcc 3.3 V.
5. See TC values in Figure 20 on page 27 for approximate Rp value and TC.

Figure 17. tFall and tRise (V_{CCQ} = 1.7-1.95V)



Notes:
1. tFALL is VOH(DC) to VOL(AC) and tRISE is VOL(DC) to VOH(AC).
2. tRise is primarily dependent on external pull-up resistor and external capacitive loading.
3. tFall . 7ns at 1.8V.
4. See TC values in Figure 20 on page 27 for TC and approximate Rp value.

Figure 18. IOL versus Rp (V_{CCQ} = 2.7-3.6V)

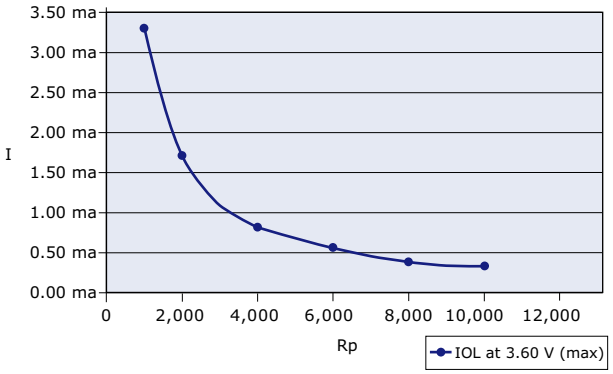


Figure 19. IOL versus Rp (V_{CCQ} = 1.7-1.95V)

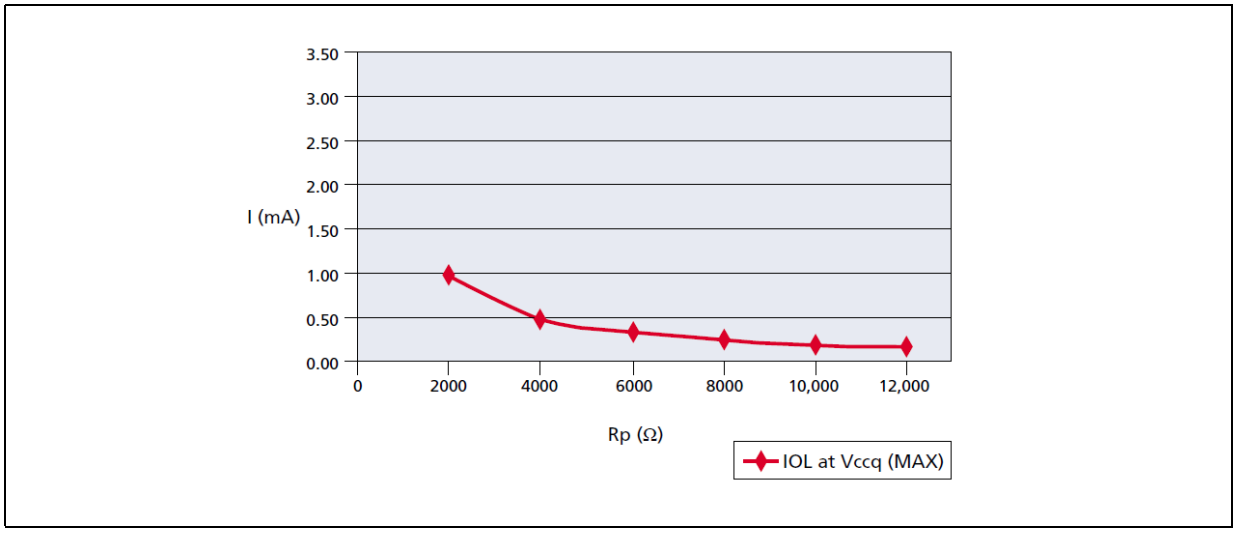
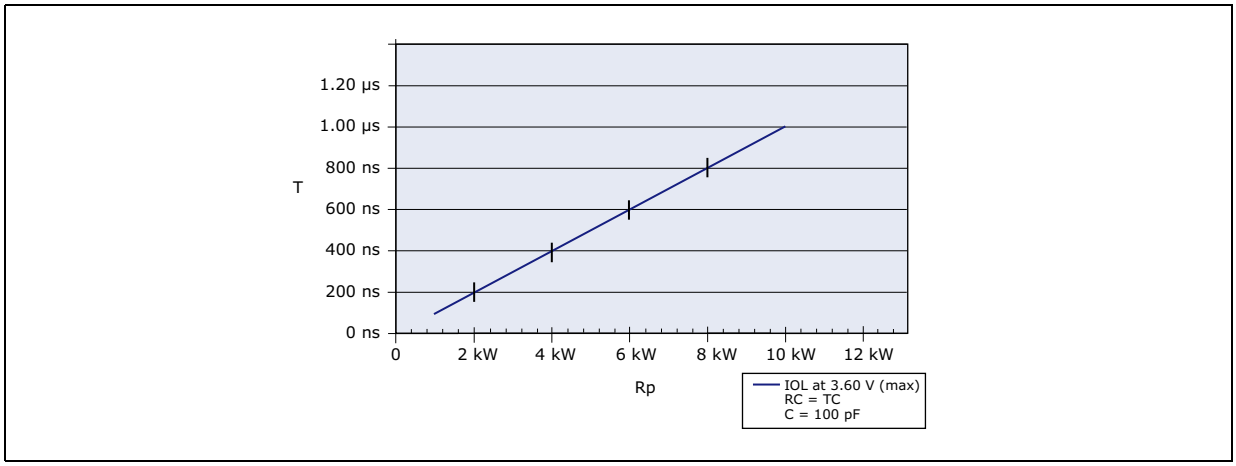


Figure 20. TC versus Rp



6.0 Bus Operation — Synchronous Interface (ONFI 2.3)

These NAND Flash devices have two interfaces—a synchronous interface for fast data (synchronous) I/O transfer and an asynchronous interface that is backward compatible with existing NAND Flash devices.

The NAND Flash command protocol for both the asynchronous and synchronous interfaces is identical. However, there are some differences between the asynchronous and synchronous interfaces when issuing command, address, and data I/O cycles using the NAND Flash signals.

When the synchronous interface is activated on a target (see Section 9.0, “Activating Interfaces” on page 55), the target is capable of high-speed synchronous data transfers. Existing signals are redefined for high-speed synchronous I/O. The WE# signal becomes CLK. DQS is enabled. The RE# signal becomes W/R#. CLK provides a clock reference to the NAND Flash device.

DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

The direction of DQS and DQ[7:0] is controlled by the W/R# signal. When the W/R# signal is latched HIGH, the controller is driving the DQ bus and DQS. When the W/R# is latched LOW, the NAND Flash is driving the DQ bus and DQS.

Transition from the synchronous ONFI 2.3 interface to the synchronous ONFI 3.0 interface is not permitted.

The synchronous interface bus modes are summarized below.

Table 4. Synchronous ONFI 2.3 Interface Mode Selection

Mode	CE#	CLE	ALE	CLK	W/R#	DQS	DQ[7:0]	WP#	Notes
Standby	H	X	X	X	X	X	X	0 V/Vccq	1, 2
Bus Idle	L	L	L		H	X	X	X	
Bus driving	L	L	L		L	output	output	X	
Command Input	L	H	L		H	X	input	H	3
Address Input	L	L	H		H	X	input	H	3
Data Input	L	H	H		H		input	H	4
Data Output	L	H	H			Note 5	output	X	5

Table 4. Synchronous ONFI 2.3 Interface Mode Selection

Mode	CE#	CLE	ALE	CLK	W/R#	DQS	DQ[7:0]	WP#	Notes
Write Protect	X	X	X	X	X	X	X	L	
Undefined	L	L	H		L	output	output	X	
Undefined	L	H	L		L	output	output	X	

Notes:
1. CLK can be stopped when the target is disabled, even when R/B# is LOW.
2. WP# should be biased to CMOS LOW or HIGH for standby.
3. Commands and addresses are latched on the rising edge of CLK.
4. During data input to the device, DQS is the “clock” that latches the data in the cache register.
5. During data output from the NAND Flash device, DQS is an output generated from CLK after tDQSCK delay.
6. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

6.1 Synchronous ONFI 2.3 Enable/Standby

In addition to the description found in Asynchronous Enable/Standby, the following requirements also apply when the synchronous interface is active.

Before enabling a target, CLK must be running and ALE and CLE must be LOW. When CE# is driven LOW, all of the signals for the selected target are enabled. The target is not enabled until tCS completes; the target's bus is then idle.

Prior to disabling a target, the target's bus must be idle. A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#. After the target is disabled, CLK can be stopped.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations.

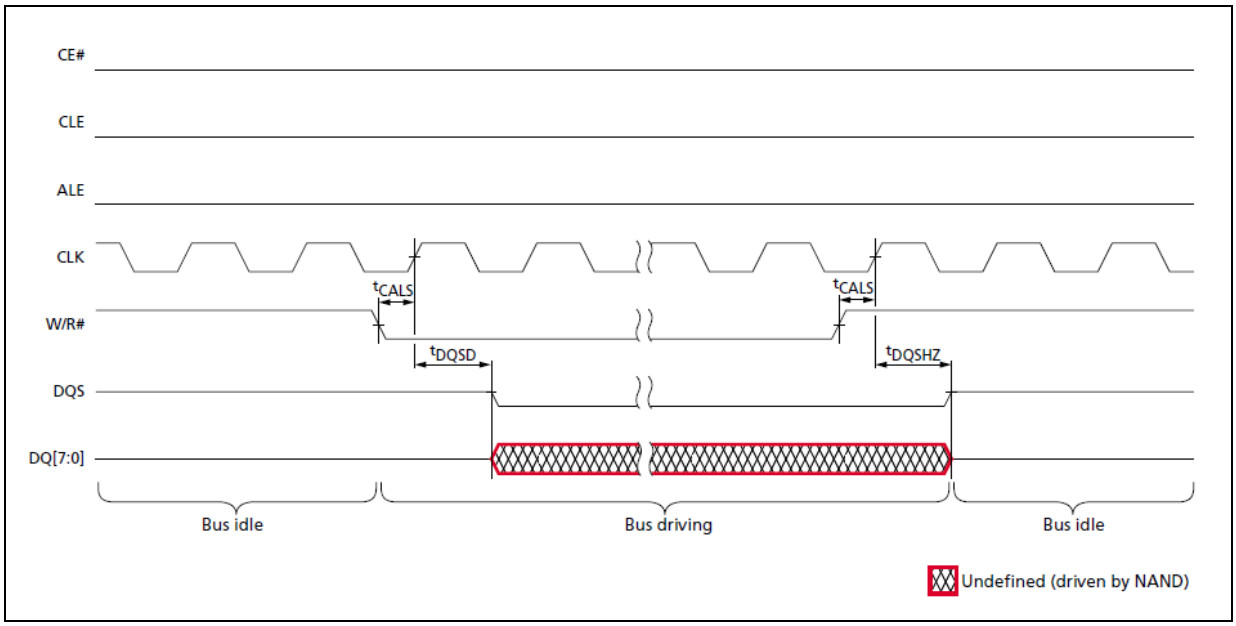
6.2 Synchronous ONFI 2.3 Bus Idle / Driving

A target's bus is idle or driving when CLK is running, CE# is LOW, ALE is LOW, and CLE is LOW.

The bus is idle when W/R# transitions HIGH and is latched by CLK. During the bus idle mode, all signals are enabled; DQS and DQ[7:0] are inputs. No commands, addresses, or data are latched into the target; no data is output. When entering the bus idle mode, the host must wait a minimum of ^{t}CAD before changing the bus mode. In the bus idle mode, the only valid bus modes supported are: bus driving, command, address, and onfi 2.3 data input.

The bus is driving when W/R# transitions LOW and is latched by CLK. During the bus driving mode, all signals are enabled; DQS is LOW and DQ[7:0] is driven LOW or HIGH, but no valid data is output. Following the bus driving mode, the only valid bus modes supported are bus idle and synchronous data output.

Figure 21. Onfi 2.3 Bus Idle / Driving Behavior



Note: 1. Only the selected die (LUN) drives DQS and DQ[7:0]. During an interleaved die (multi- LUN) operation, the host must use the READ STATUS ENHANCED (78h) to prevent data output contention.

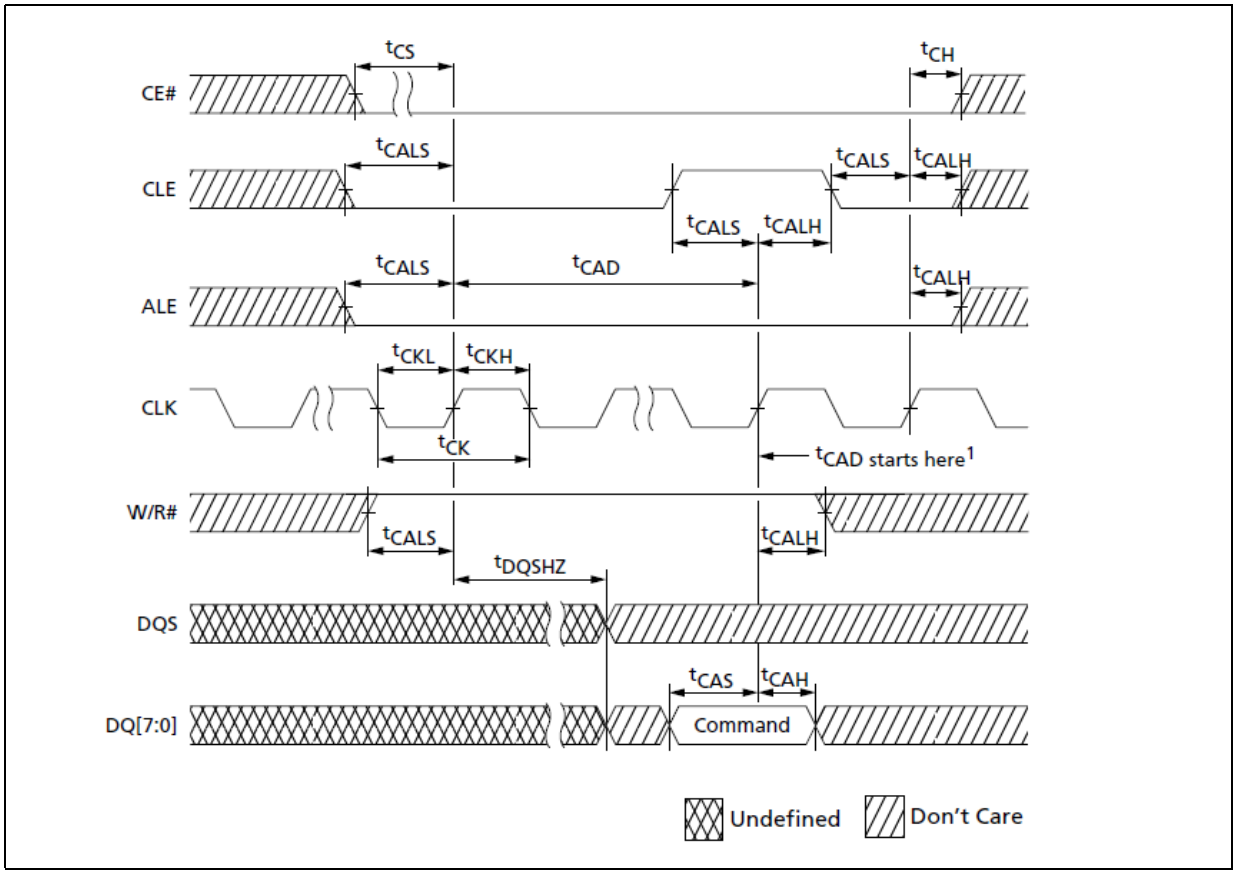
6.3 Synchronous ONFI 2.3 Commands

A command is written from DQ[7:0] to the command register on the rising edge of CLK when CE# is LOW, ALE is LOW, CLE is HIGH, and W/R# is HIGH.

After a command is latched—and prior to issuing the next command, address, or data I/O—the bus must go to bus idle mode on the next rising edge of CLK, except when the clock period, ^{t}CK, is greater than ^{t}CAD.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, such as READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs), even when they are busy.

Figure 22. Synchronous ONFI 2.3 Command Cycle



Note: When CE# remains LOW, tCAD begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

6.4 Synchronous ONFI 2.3 Addresses

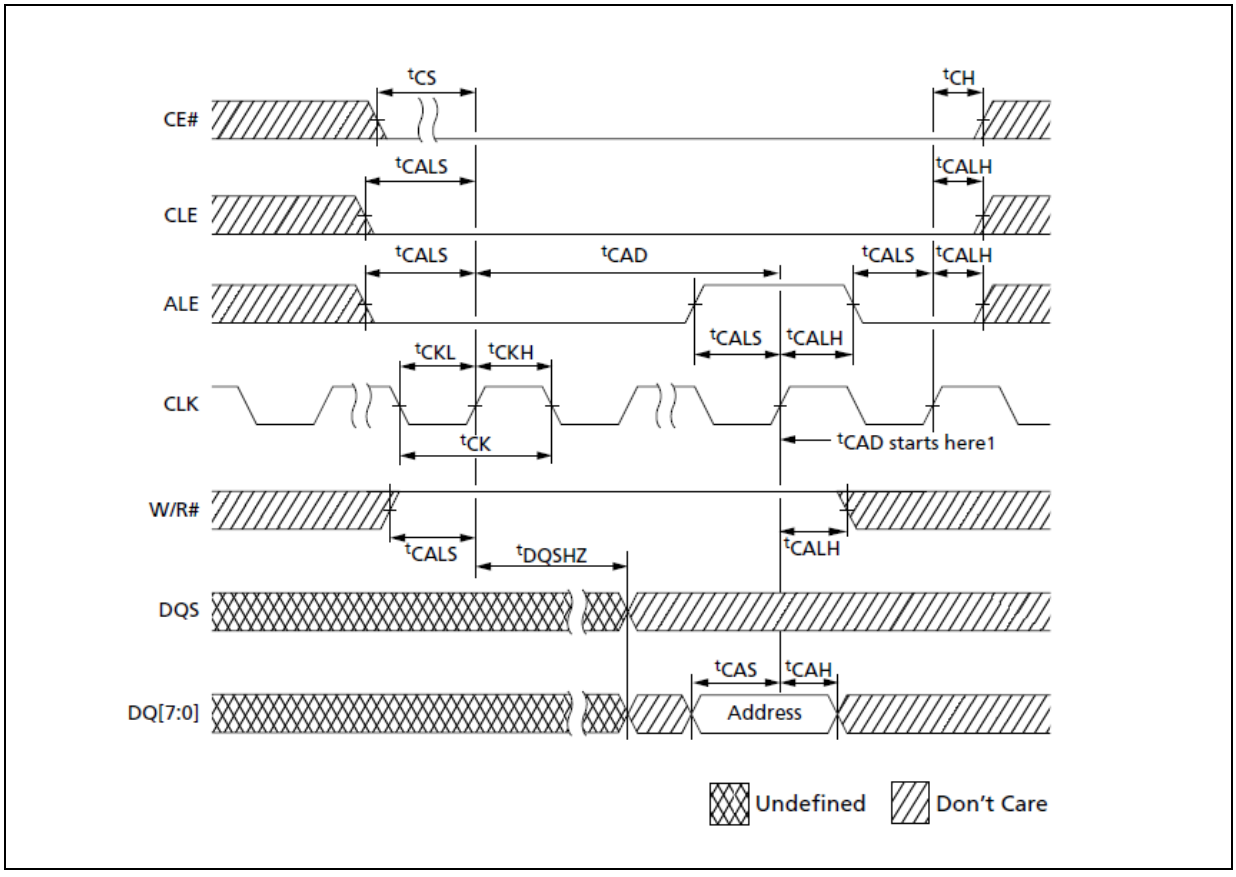
A synchronous address is written from DQ[7:0] to the address register on the rising edge of CLK when CE# is LOW, ALE is HIGH, CLE is LOW, and W/R# is HIGH.

After an address is latched—and prior to issuing the next command, address, or data I/O—the bus must go to bus idle mode on the next rising edge of CLK, except when the clock period, ^{t}CK, is greater than ^{t}CAD.

Bits not part of the address space must be LOW (see Section 4.0, “Array Organization” on page 16). The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements.

Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses such as address cycles that follow the READ STATUS ENHANCED (78h) command, are accepted by die (LUNs), even when they are busy.

Synchronous ONFI 2.3 Address Cycle



Note: When CE# remains LOW, tCAD begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

6.5 Synchronous ONFI 2.3 Data Input

To enter the synchronous data input mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- W/R# is HIGH
- ^{t}CAD is met
- DQS is LOW
- ALE and CLE are HIGH on the rising edge of CLK

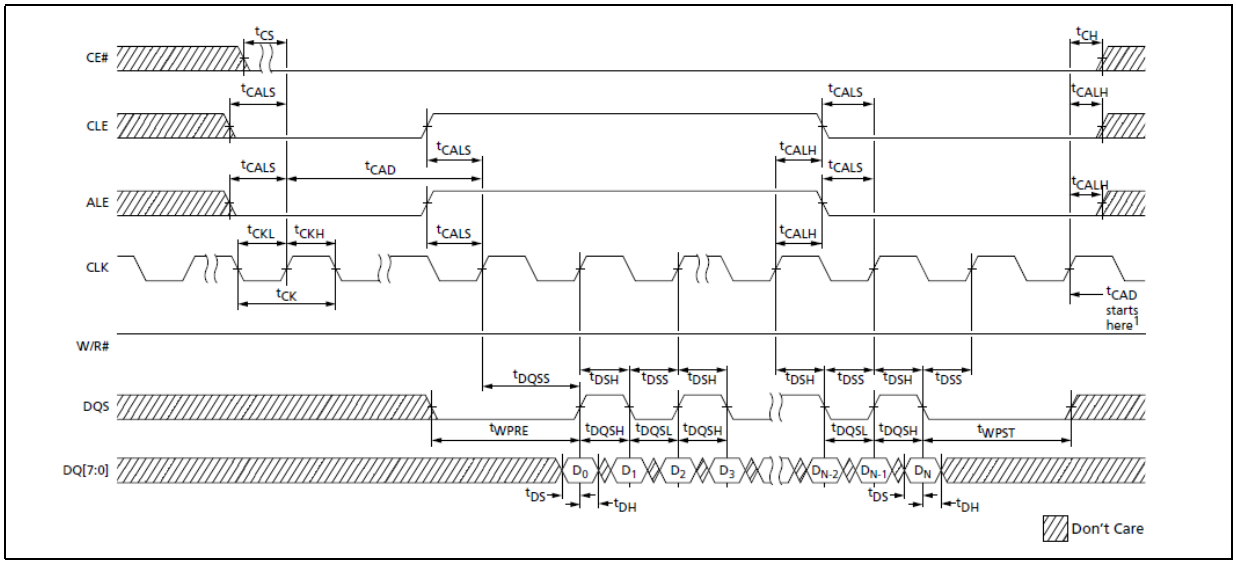
Upon entering the onfi 2.3 data input mode after ^{t}DQSS, data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when CLK is running and the DQS to CLK skew meets ^{t}DSH and ^{t}DSS, CE# is LOW, W/R# is HIGH, and ALE and CLE are HIGH on the rising edge of CLK.

To exit synchronous data input mode, the following conditions must be met:

- CLK is running and the DQS to CLK skew meets ^{t}DSH and ^{t}DSS
- CE# is LOW
- W/R# is HIGH
- ALE and CLE are latched LOW on the rising edge of CLK
- The final two data bytes of the data input sequence are written to DQ[7:0] to the cache register on the rising and falling edges of DQS after the last cycle in the data input sequence in which ALE and CLE are latched HIGH.
- DQS is held LOW for ^{t}WPST (after the final falling edge of DQS)

Following ^{t}WPST, the bus enters bus idle mode and ^{t}CAD begins on the next rising edge of CLK. After ^{t}CAD starts, the host can disable the target if desired. Data input is ignored by die (LUNs) that are not selected or are busy.

Figure 23. Synchronous ONFI 2.3 Data Input Cycles



Notes:
1. When CE# remains LOW, ^{t}CAD begins at the first rising edge of the clock after ^{t}WPST completes.
2. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
3. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).

6.6 Synchronous ONFI 2.3 Data Output

Data can be output from a die (LUN) if it is ready. Data output is supported following a READ operation from the NAND Flash array.

To enter the synchronous data output mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- The host has released the DQ[7:0] bus and DQS
- W/R# is latched LOW on the rising edge of CLK to enable the selected die (LUN) to take ownership of the DQ[7:0] bus and DQS within ^{t}WRCK
- ^{t}CAD is met
- ALE and CLE are HIGH on the rising edge of CLK

Upon entering the synchronous data output mode, DQS will toggle HIGH and LOW with a delay of ^{t}DQSCK from the respective rising and falling edges of CLK. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than ^{t}AC.

Synchronous data output mode continues as long as CLK is running, CE# is LOW, W/R# is LOW, and ALE and CLE are HIGH on the rising edge of CLK.

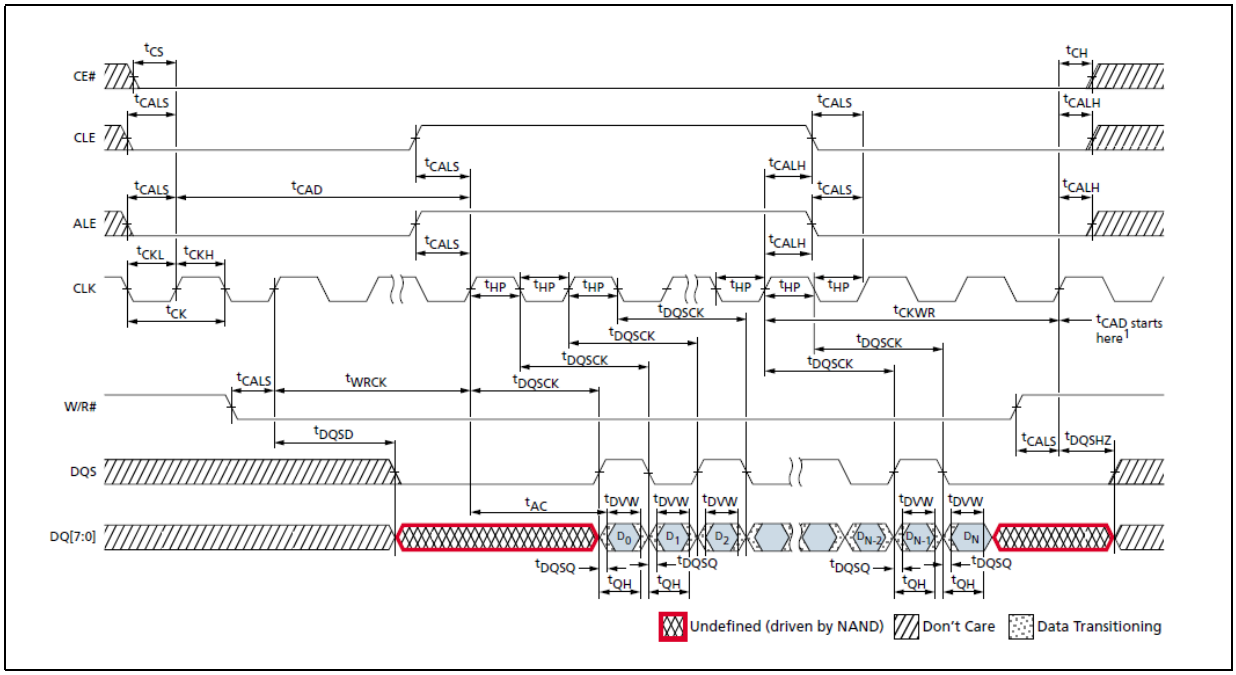
To exit synchronous data output mode, the following conditions must be met:

- CLK is running
- CE# is LOW
- W/R# is LOW
- ALE and CLE are latched LOW on the rising edge of CLK

The final two data bytes are output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur ^{t}DQSCK after the last cycle in the data output sequence in which ALE and CLE are latched HIGH. After ^{t}CKWR, the bus enters bus idle mode and ^{t}CAD begins on the next rising edge of CLK. Once ^{t}CAD starts the host can disable the target if desired.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

Figure 24. Synchrnous ONFI 2.3 Data Output Cycles



Notes:

1. When CE# remains LOW, ^{t}CAD begins at the rising edge of the clock after ^{t}CKWR for subsequent command or data output cycle(s).
2. See Figure 23 on page 33 for details of W/R# behavior.
3. ^{t}AC is the DQ output window relative to CLK and is the long-term component of DQ skew.
4. For W/R# transitioning HIGH, DQ[7:0] and DQS go to tri-state.
5. For W/R# transitioning LOW, DQ[7:0] drives current state and DQS goes LOW.
6. After final data output, DQ[7:0] is driven until W/R# goes HIGH, but is not valid.

6.7 Write Protect

See "Write Protect" in Section 5.0, "Bus Operation — Asynchronous Interface" on page 17.

6.8 Ready/Busy#

See "Ready/Busy#" in Section 5.0, "Bus Operation — Asynchronous Interface" on page 17.

7.0 Bus Operation — Synchronous ONFI 3.0 Interface

When the synchronous ONFI 3.0 interface is activated on a target (see "Activating Interfaces" on page 55), the target is capable of high-speed DDR data transfers. and the DQS signal is enabled. DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

For operations in synchronous ONFI 3.0 mode, the synchronous interface must be selected (see "Activating Interfaces" on page 55). The features that synchronous ONFI 3.0 operations offer beyond synchronous ONFI 2.3 operations include:

- Supported only at 1.8V V_{CCQ}
- Support for speeds beyond 200MT/s
- Support for differential signaling for the RE# and/or DQS signals (RE_c, DQS_c)
- Support for Warmup Cycles
- Support for On-die Termination (ODT)
- Support for V_{REFQ}

Use of differential signaling is optional, however devices tested in synchronous mode are with differential signaling enabled which is needed to guarantee AC timings in the synchronous mode. If not using the differential signaling, statements about those signal types can be ignored.

Transition from the synchronous ONFI 3.0 interface to the synchronous ONFI 2.3 interface is not permitted.

The synchronous ONFI 3.0 interface bus modes are summarized below:

Table 5. Synchronous ONFI 3.0 Interface Mode Selection

Mode	CE#	CLE	ALE	RE# (RE_t)	DQS (DQS_t)	DQ[7:0]	WE#	WP#	Notes
Standby	H	X	X	X	X	X	X	0 V/Vccq	1, 2
Idle	L	L	L	H	H	X	H	X	5
Command Input	L	H	L	H	H	input		H	3
Address Input	L	L	H	H	X	input		H	3
Data Input	L	L	L	H		input	H	H	2,3
Data Output	L	L	L			outpu	H	X	2,3,4
Write Protect	X	X	X	X	X	X	X	L	

Notes:
1. The current state of the device is data input, data output, or neither based on the commands issued.
2. There are two data input/output cycles from the rising edge of DQS/RE# to the next rising edge of DQS/RE#.
3. ODT may be enabled as part of the data input and data output cycles.
4. At the beginning of a data output burst, DQS shall be held HIGH for ^{t}DQSRH after RE# transitions LOW to begin data output.
5. WE# is set HIGH during the Idle state.
6. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

7.1 Differential Signaling

An enabler for higher speed operation is differential signaling for the RE# and DQS signals. A complementary RE# and complementary DQS signal may be optionally used to create differential signal pairs (RE_t/RE_c and DQS_t/DQS_c). When using differential signaling, RE# is referred to as RE_t and DQS is referred to as DQS_t, i.e., the "true" versions of the signals. Differential signaling may be used to improve signal integrity through enhanced noise immunity. Differential signaling shall only be enabled for use when the synchronous ONFI 3.0 data interface is selected.

A device may support differential RE# and/or differential DQS signaling. The support for differential RE# and/or DQS is reported in the parameter page. Complementary RE# (i.e., RE_c) and complementary DQS (i.e., DQS_c) signals are individually configured/enabled. By default, differential signaling is disabled. The host may configure the device to use differential signaling using the synchronous ONFI 3.0 Configuration feature address.

To begin using differential signaling, the host shall issue a SET FEATURES (EFh) command to the Timing Mode feature address that sets the Data Interface from asynchronous to synchronous ONFI 3.0 operation. Then issue a SET FEATURES (EFh) command to the synchronous ONFI 3.0 Configuration feature address to activate differential RE# and/or differential DQS signaling. The differential signaling is then enabled after CE# is brought HIGH.

To change from differential signaling to single-ended signaling, the host shall configure the device using the synchronous ONFI 3.0 Configuration feature address to disable differential signaling. The differential signaling is disabled after CE# is brought HIGH.

A RESET (FFh) command will disable differential signaling. The SYNCHRONOUS RESET (FCh) and RESET LUN (FAh) commands have no effect on differential signaling.

7.2 Warmup Cycles

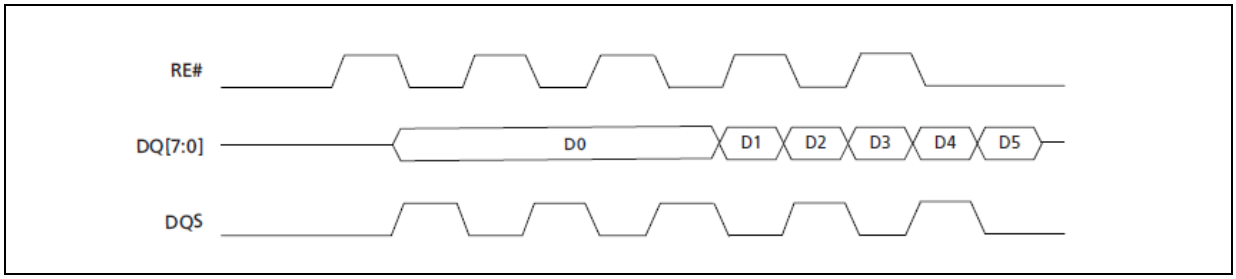
To support higher speed operation, warmup cycles for data output and data input may be provided. Warmup cycles shall only be enabled for use when the synchronous ONFI 3.0 data interface is selected.

Warmup cycles for data output provides extra RE# and corresponding DQS transitions at the beginning of a data output burst. These extra RE#/DQS transitions do not have any data associated with them. The number of extra cycles is configured via the synchronous ONFI 3.0 Configuration feature address.

Warmup cycles for data input provides extra DQS transitions at the beginning of a data input burst. These extra DQS transitions do not have any data associated with them. The number of extra cycles is configured via the synchronous ONFI 3.0 Configuration feature address. The number of cycles specified includes a full data input cycle (both rising and falling edge for DQS).

Warmup cycles are optional for both data output and data input, and if used, do not need to be configured to the same value. Warmup cycles apply to all commands. Warmup cycles are initiated at the start of each data burst when warmup cycles are enabled for that data transfer type. If the host pauses and then resumes a data transfer without exiting and re-entering the data burst, then the host shall not issue additional warmup cycles. Exiting and re-entering the data burst shall be performed by bringing ALE, CLE, or CE# HIGH without latching with WE#. In the case of not re-issuing warmup cycles, the host should take care to avoid signal integrity issues due to pausing the data transfer and resuming without warmup cycles.

Figure 25. Warmup Cycles for data output (2 warmup cycles)



7.3 On-die Termination (ODT)

On-die termination may be required at higher speeds depending on system topology. On-die termination applies to the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals. On-die termination is an optional capability that may be employed to meet higher speeds in particular topologies. If power needs to be optimized in a particular condition, then on-die termination may be disabled and the topology may be run at a slower timing mode. On-die termination shall only be enabled for use in the synchronous ONFI 3.0 data interface.

On-die termination settings are configured during device initialization. The host may configure the ODT in a self-termination only configuration, or matrix termination which enables a combination of Target and non-Target termination to be specified.

For the more flexible matrix termination the host configures a matrix that defines the LUN(s) that terminate for a particular Volume. This matrix is configured using the ODT CONFIGURE (E2h) command. After the on-die termination matrix is defined, ODT is enabled and disabled based on the type of cycle (on for data input and output cycles, off for command, and address cycles). On-die termination applies for data input and output cycles for all command types, including both single data rate (SDR) and double data rate (DDR) transfers.

Volume addressing is required for use of non-target on-die termination (ODT) functionality. See Section 14.0, “Configuration Operations” on page 73 for how to appoint volume addresses. Once volume addresses have been appointed they can be selected with the VOLUME SELECT (E1h) command. For target only termination, no ODT termination matrix is required.

The on-die termination configuration matrix and control mechanism utilize Volume addresses. Volume addressing is a required capability to utilize non-Target on-die termination.

When on-die termination is enabled via the synchronous ONFI 3.0 Configuration feature address, the default is Target termination. For non-Target termination or termination topologies that use multiple terminators, the Volume address mechanism shall be used and the on-die termination configuration matrix shall be specified using the ODT CONFIGURE (E2h) command. As part of the ODT CONFIGURE (E2h) command, RTT settings may be specified on a per LUN basis with individual values for:

- RE#
- DQ[7:0] and DQS for data output
- DQ[7:0] and DQS for data input

On-die termination is enabled when ALE, CLE and CE# transition from HIGH to LOW.

On-die termination is disabled when ALE, CLE or CE# transitions from LOW to HIGH.

Table 6. On-die Termination DC Electrical Characteristics

Mode	Symbol	Min	Typ	Max	Units	Notes
R_{TT} effective impedance value for 50 Ohm setting	$R_{TT\ 2\ (EFF)}$	32.5	50	67.5	Ohms	1
R_{TT} effective impedance value for 75 Ohm setting	$R_{TT\ 3(EFF)}$	48.7	75	101.3	Ohms	1
R_{TT} effective impedance value for 100 Ohm setting	$R_{TT\ 4(EFF)}$	65	100	135	Ohms	1
R_{TT} effective impedance value for 150 Ohm setting	$R_{TT\ 5(EFF)}$	97.5	150	202.5	Ohms	1
Deviation of VM with respect to VCCQ/2	$VM\Delta$	-	-	7	Percent	2

Notes:

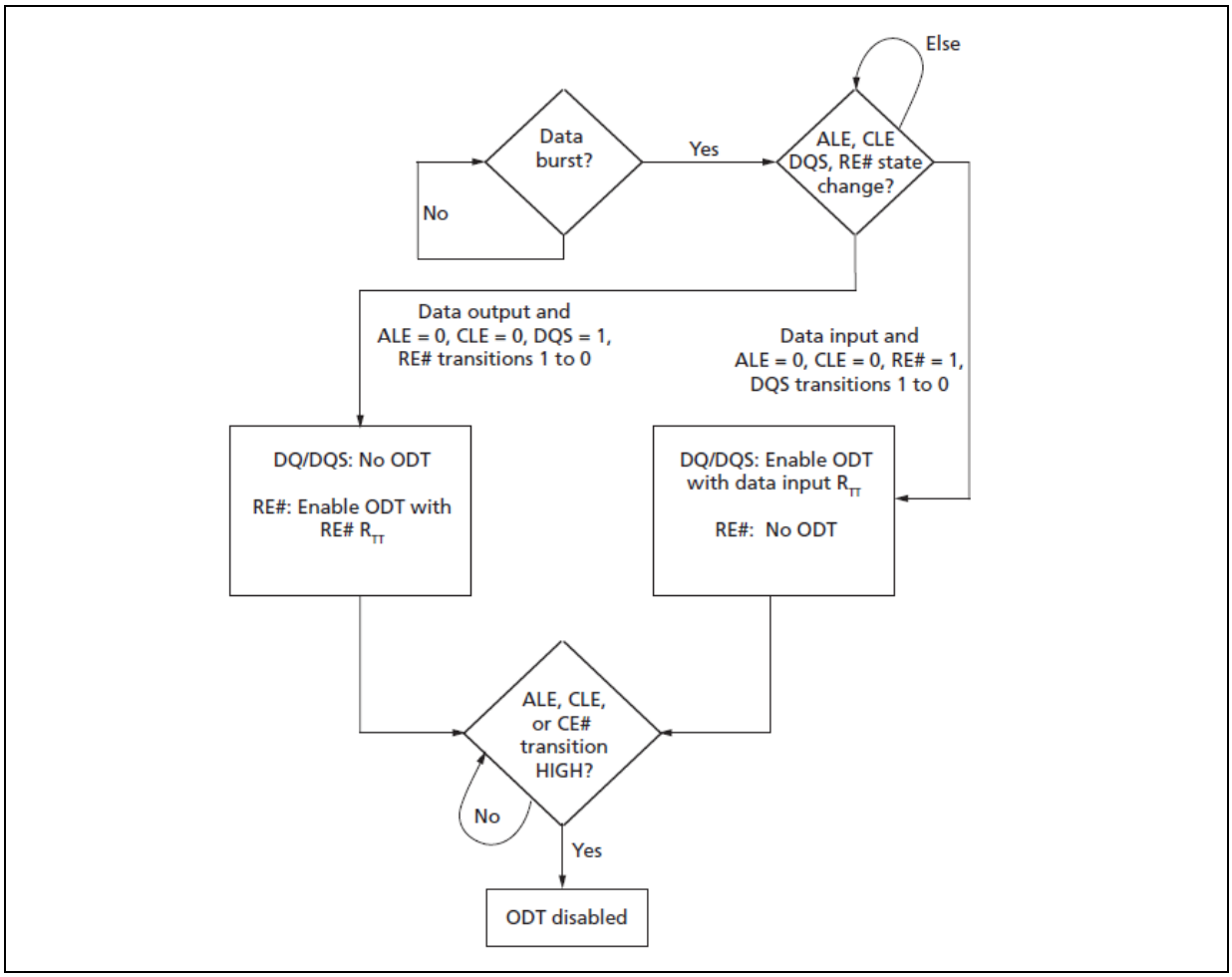
1. $R_{TT2\ (EFF)}$, $R_{TT3\ (EFF)}$, $R_{TT4\ (EFF)}$, and $R_{TT5\ (EFF)}$ are determined by separately applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to the signal being tested, and then measuring current $I(V_{IH[AC])}$ and $I(V_{IL[AC]})$, respectively. $R_{TT(EFF)} = (V_{IH[AC]} - V_{IL[AC]}) / (I(V_{IH[AC]}) - I(V_{IL[AC]})$
2. Measure voltage (VM) at the tested signal with no load. $VM\Delta = [(2 \times VM) / V_{CCQ}] \times 100$.

7.4 Self-termination On-die Termination (ODT)

When self-termination is enabled, the LUN that is executing the command provides ondie termination. Figure 26 defines the self-termination only ODT enable and disable requirements for the LUN that is executing the command when ODT is selected for use via SET FEATURES (EFh) command. If the ODT CONFIGURE (E2h) command is issued to a LUN on a Target, then the ODT mechanism used for that Target changes to matrix termination.

Self-termination is applied to DQS and DQ[7:0] singals during data input operations and RE# during data output operations.

Figure 26. Self-termination only ODT behavioral flow



7.5 Matrix Termination

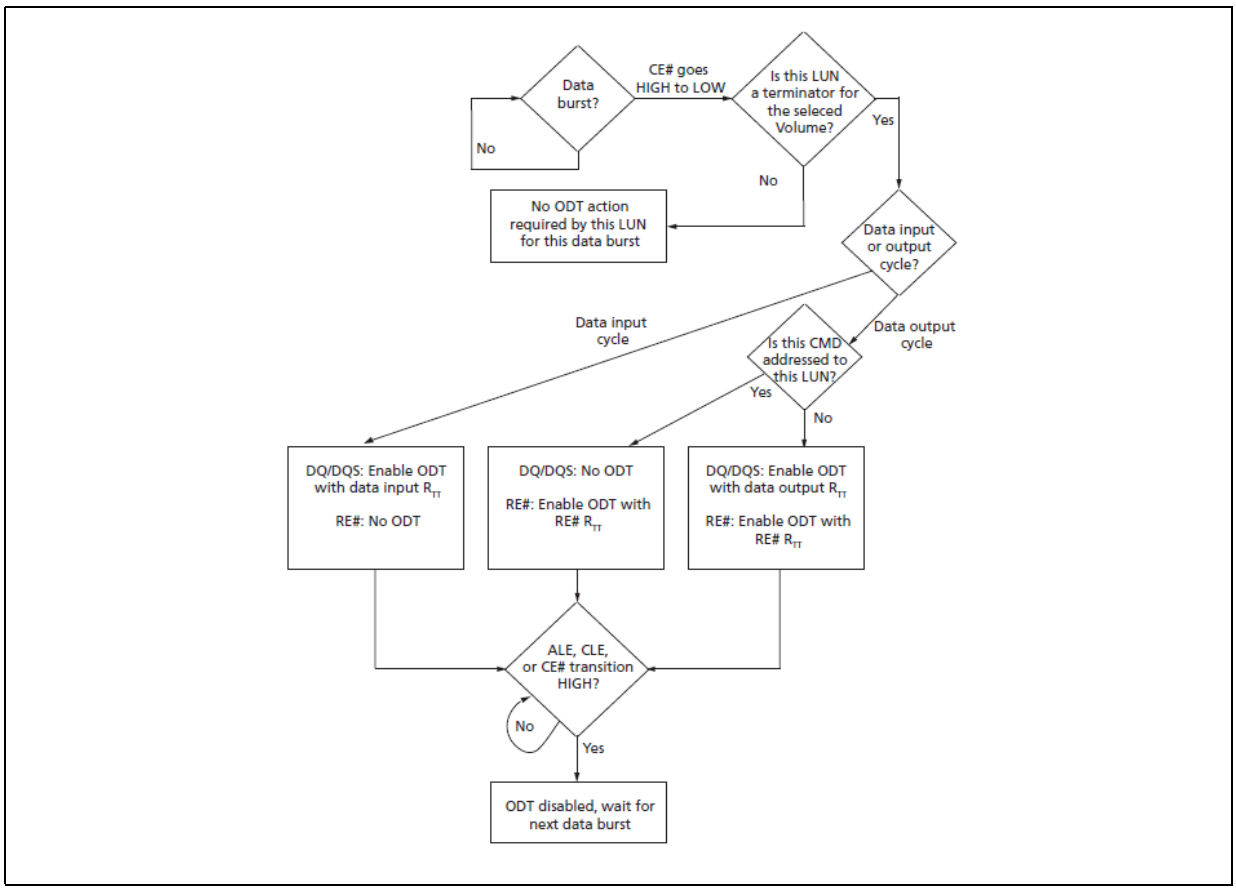
A LUN that is configured to act as a terminator using the configuration matrix (that is specified with the ODT CONFIGURE (E2h) command) may be located on the selected Volume as the Volume it is terminating for (Target termination) or a unselected Volume (non-Target termination). Based on the ODT configuration and the Volume a command is addressed to, LUNs enter different states which determine their ODT behavior; those states are listed in Table 7.

Table 7. LUN state for Matrix Termination

LUN is on selected Volume?	Terminator for selected Volume?	LUN state	ODT actions defined
Yes	N/A	Selected	Figure 27
No	Yes	Sniff	Figure 28
No	No	Deselected	No ODT actions

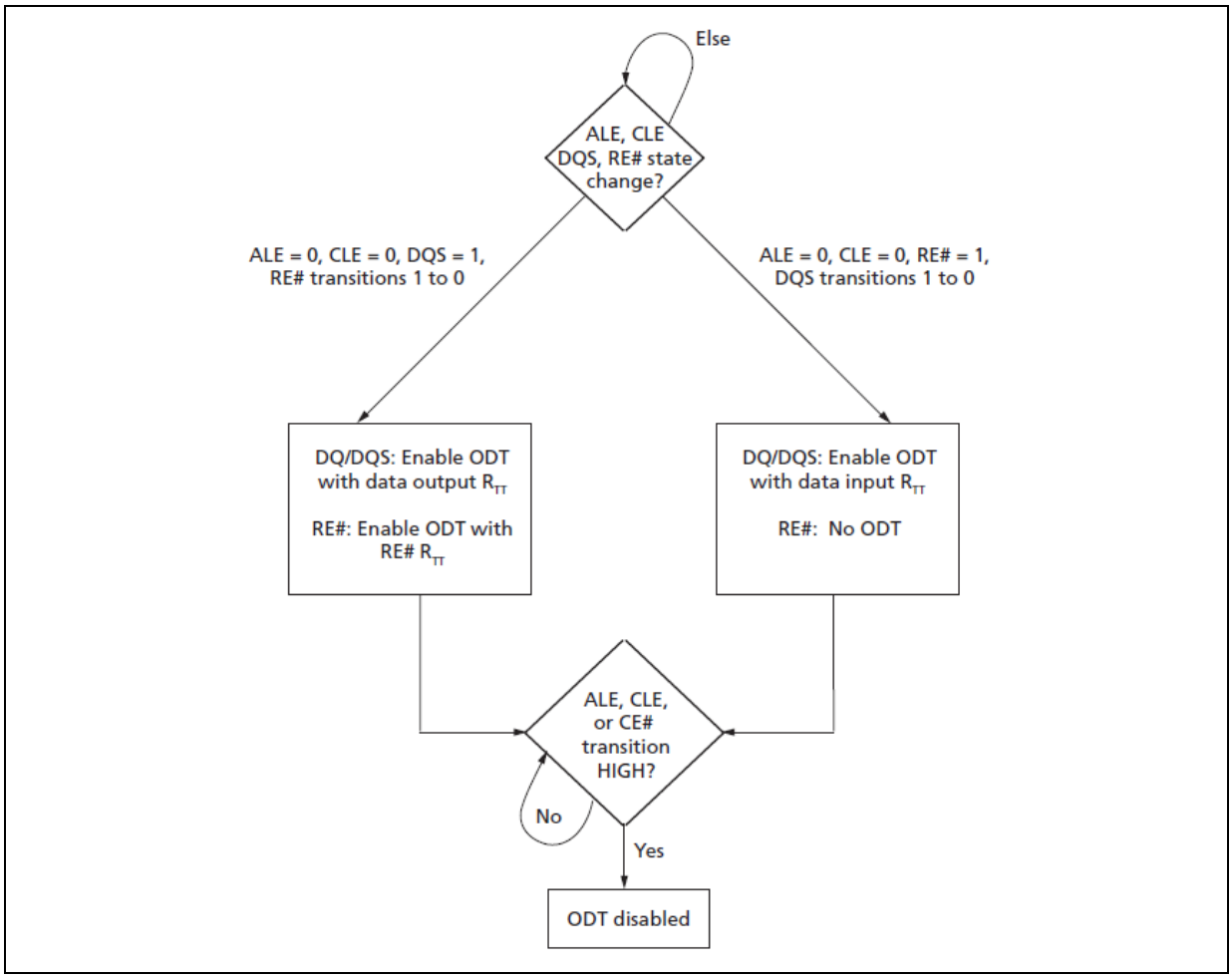
A LUN which a command is issued to for execution may provide termination. Other LUNs on the selected Volume that are not responsible for execution of the command may also provide termination. Figure 27 defines the ODT actions required for LUNs of each of these types on the selected Volume. LUNs on the selected Volume remain in an active state, and thus are aware of state information such as whether there is a data burst currently and the type of cycle; these LUNs do not rely only on ALE, CLE, DQS and RE# signals.

Figure 27. ODT actions for LUNs on selected Volume



The ODT configuration matrix also offers the flexibility of having LUNs on an unselected Volume provide termination for the selected Volume. When a LUN is placed in the Sniff state, it checks the ALE, CLE, DQS and RE# signals to determine when to enable or disable ODT. Figure 28 defines the ODT actions for LUNs in the Sniff state on an unselected Volume.

Figure 28. ODT actions for LUNs in Sniff state on unselected Volume



7.5.1 Matrix Termination Examples

This section describes two examples of on-die termination configurations using matrix termination. In both examples, each Volume consists of two LUNs, referred to as H0N*n*-LUN0 and H0N*n*-LUN1. The following Volume addresses were appointed at initialization.

Table 8. Volume appointment for Matrix Termination example

Volume	Appointed Volume Address
H0N0	0
H0N1	1
H0N2	2
H0N3	3

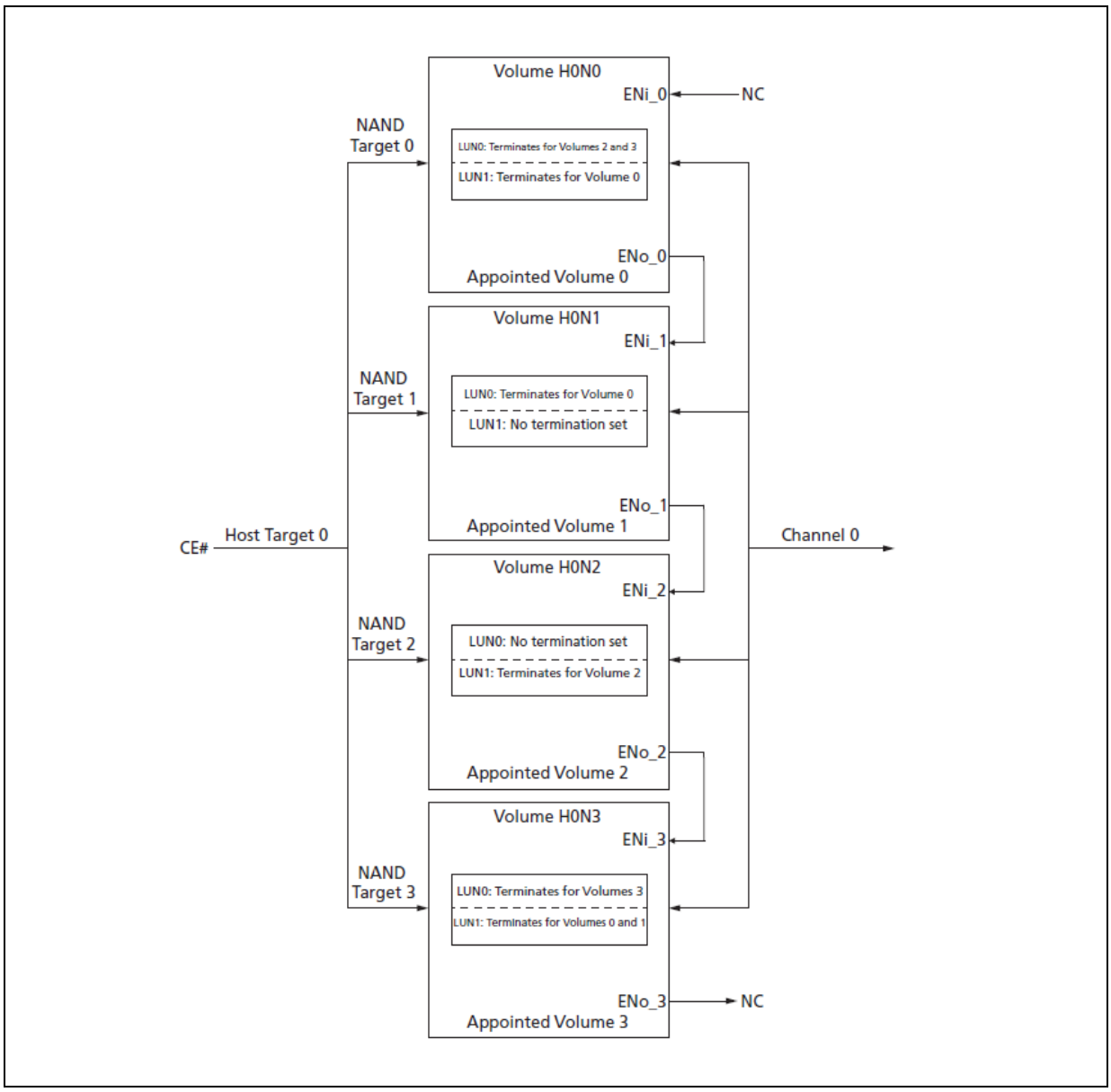
For optimal signal integrity and power consumption, the host may configure termination in a variety of ways. The host may configure a LUN to self terminate, perform non-Target termination for another Volume, or not perform any termination function. Using matrix termination, the termination R_{TT} values may be set differently for each LUN configured as a terminator, including the ability to specify different settings for data output operation and data input operation. The first example shows that a controller may configure the ODT matrix to perform stronger non-Target ODT for data output operations and weaker Target ODT for data input operations.

Table 9. Non-Target ODT for Data Output, Target ODT for Data Input settings configuration example

	Input values for ODT CONFIGURE (E2h)				
LUN	Byte M0	Byte M1	Byte R_{TT1}	Byte R_{TT2}	Notes
H0N0-LUN0	0Ch	00h	40h	00h	Terminates for Volumes 2 and 3 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS
H0N0-LUN1	01h	00h	02h	03h	Terminates for Volume 0 (Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N1-LUN0	02h	00h	02h	03h	Terminates for Volume 1 (Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N1-LUN1	00h	00h	00h	00h	Does not act as terminator
H0N2-LUN0	00h	00h	00h	00h	Does not act as terminator
H0N2-LUN1	04h	00h	02h	03h	Terminates for Volume 2 (Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N3-LUN0	08h	00h	02h	03h	Terminates for Volume 3 (Target) for data input with an R_{TT} value of 100 Ohms for DQ[7:0]/DQS and 75 Ohms for RE#
H0N3-LUN1	03h	00h	40h	00h	Terminates for Volume 0 and 1 (non-Target) for data input with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS

Note: See Table 23, "ODT Configuration Matrix" on page 80 details on input values for ODT CONFIGURE (E2h).

Figure 29. Non-Target ODT for Data Output, Target ODT for Data Input configuration example



The second example uses parallel non-Target termination to achieve a stronger effective RTT value for both data output and data input operations.

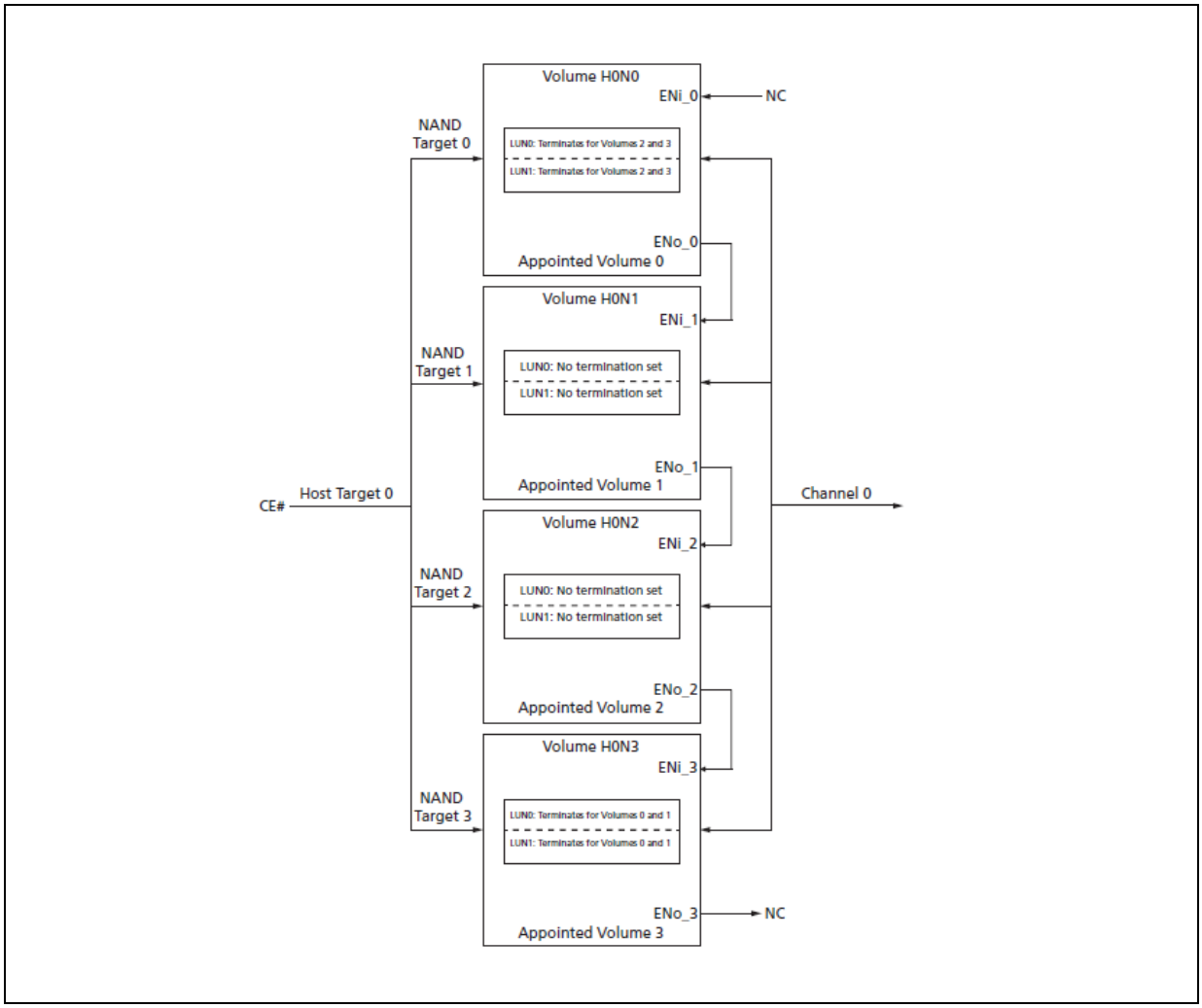
For data output, two 50 Ohm terminators are used in parallel to achieve an effective 25 Ohms non-Target termination value. For data input, two 100 Ohm terminators are used in parallel to achieve an effective 50 Ohms non-Target termination value.

This type of ODT matrix allows for stronger termination than may be available through a single device. It also allows for intermediate RTT values with the use of different RTT values for parallel LUNs. For example, if one terminator was configured for 75 Ohms and another terminator was configured for 100 Ohms for the same Volume then an effective RTT value of 43 Ohms is achieved. In this example, parallel termination is used for data input and data output for DQ[7:0]/DQS, however, RE# is non-Target terminated with 100 Ohms using a single LUN.

Table 10. Parallel Non-Target ODT settings configuration example

LUN	Input values for ODT CONFIGURE (E2h)				Notes
	Byte M0	Byte M1	Byte R_{TT1}	Byte R_{TT2}	
H0N0-LUN0	0Ch	00h	40h	00h	Terminates for Volumes 2 and 3 (non-Target) for data output with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) for data input with an RTT value of 100 Ohms for DQ[7:0]/DQS.
H0N0-LUN1	0Ch	00h	42h	01h	Terminates for Volumes 2 and 3 (non-Target) for data output with an RTT value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an RTT value of 100 Ohms for DQ[7:0]/DQS. Terminates for Volumes 2 and 3 (non-Target) with an RTT value of 150 Ohms for RE#.
H0N1-LUN0	00h	00h	00h	00h	Does not act as terminator
H0N1-LUN1	00h	00h	00h	00h	Does not act as terminator
H0N2-LUN0	00h	00h	00h	00h	Does not act as terminator
H0N2-LUN1	00h	00h	00h	00h	Does not act as terminator
H0N3-LUN0	03h	00h	42h	01h	Terminates for Volumes 0 and 1 (non-Target) for data output with an RTT value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an RTT value of 100 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) with an RTT value of 150 Ohms for RE#.
H0N3-LUN1	03h	00h	42h	00h	Terminates for Volumes 0 and 1 (non-Target) for data output with an RTT value of 50 Ohms for DQ[7:0]/DQS. Terminates for Volumes 0 and 1 (non-Target) for data input with an RTT value of 100 Ohms for DQ[7:0]/DQS.
H0N3-LUN1	03h	00h	40h	00h	Terminates for Volume 0 and 1 (non-Target) for data input with an R_{TT} value of 50 Ohms for DQ[7:0]/DQS

Figure 30. Parallel Non-Target ODT configuration example



7.6 Synchronous ONFI 3.0 Standby

Prior to disabling a target, the target's bus must be idle. A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the die (LUNs) complete their operations.

7.7 Synchronous ONFI 3.0 Idle

A target's bus is idle when CE# is LOW, ALE is LOW, CLE is LOW, RE# is HIGH, and DQS is HIGH and no internal LUN operations are ongoing or data being inputted or outputted from the target.

During the bus idle mode, all signals are enabled. No commands, addresses, or data are latched into the target; no data is output.

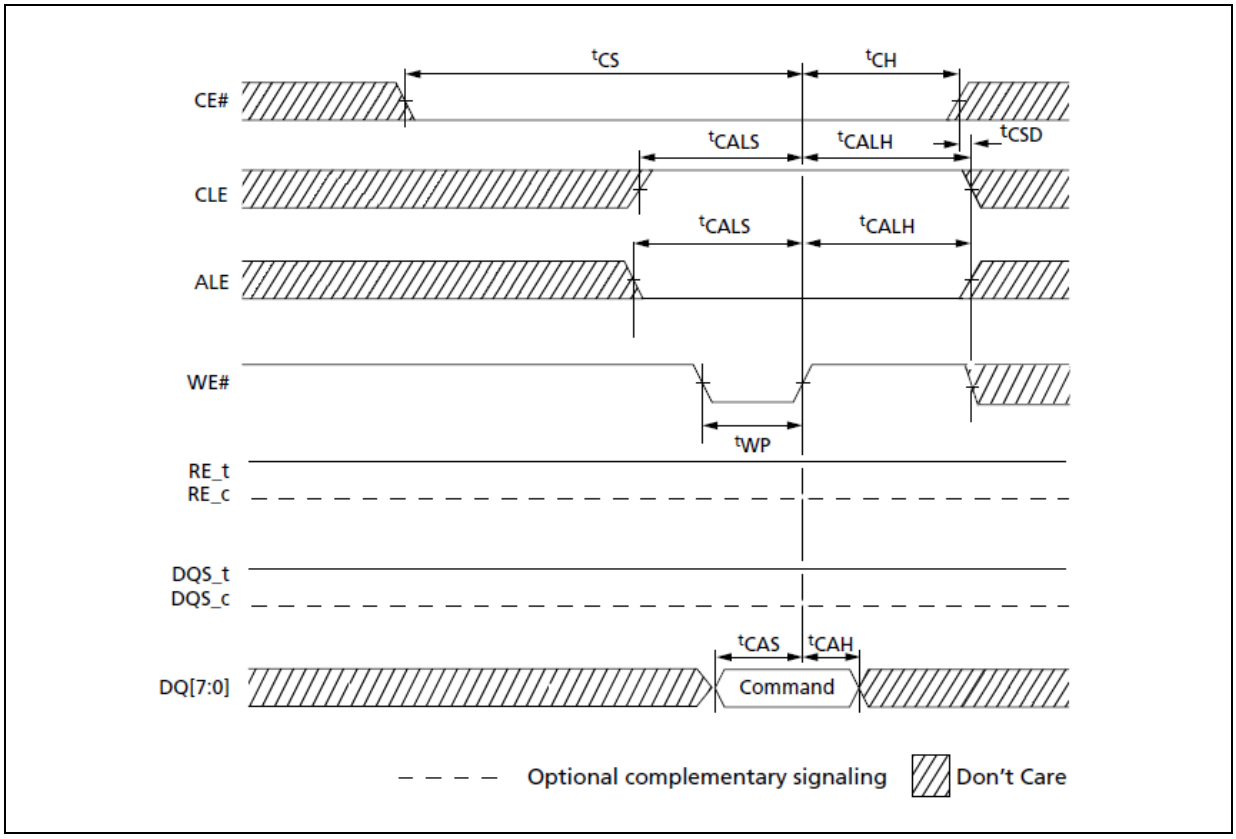
7.8 Synchronous ONFI 3.0 Commands

A command is written from DQ[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, and RE# is HIGH.

After a command is latched—and prior to issuing the next command, address, or data I/O—the bus must go to bus idle mode on the next rising edge of CLK, except when the clock period, ^{t}CK, is greater than ^{t}CAD.

Commands are typically ignored by die (LUNs) that are busy (RDY = 0); however, some commands, such as READ STATUS (70h) and READ STATUS ENHANCED (78h), are accepted by die (LUNs), even when they are busy.

Figure 31. Synchronous ONFI 3.0 Command Cycle



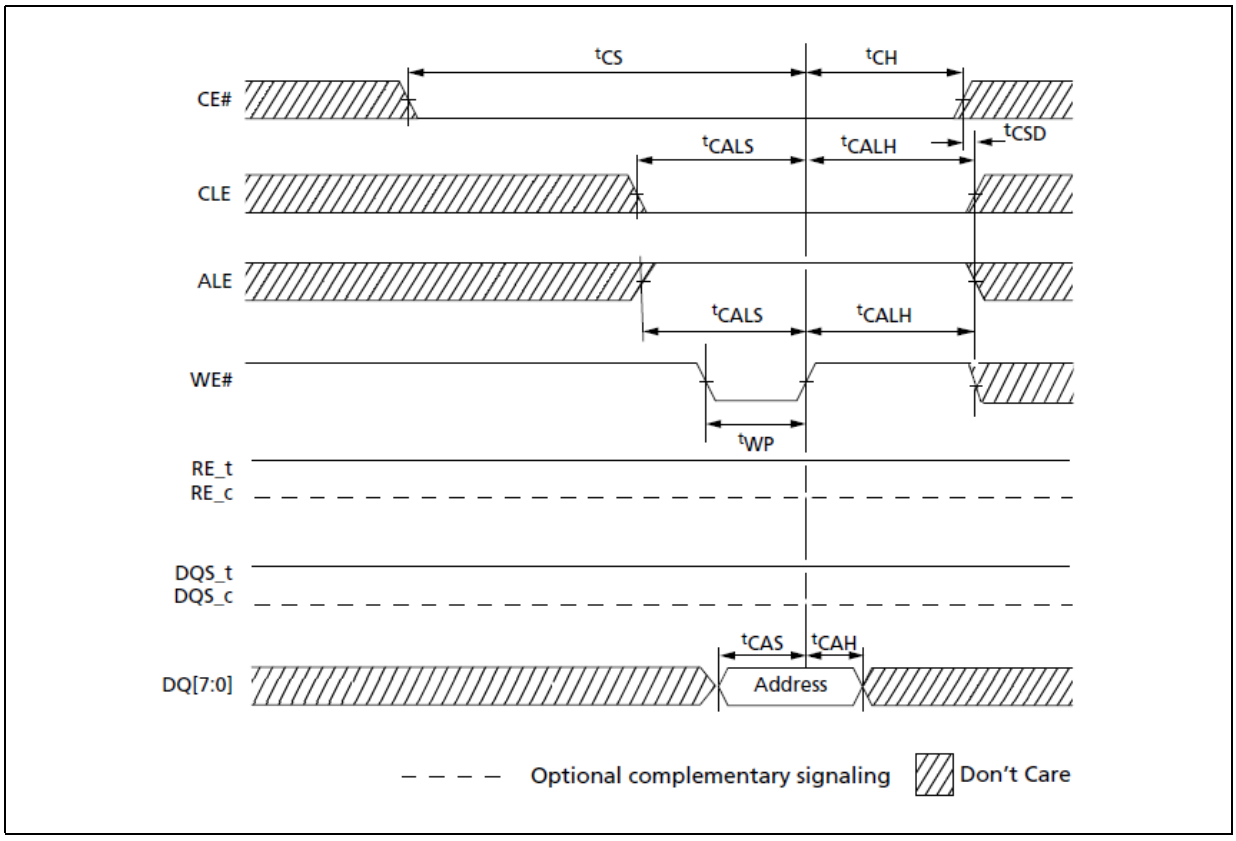
7.9 Synchronous ONFI 3.0 Addresses

A synchronous ONFI 3.0 address is written from DQ[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits not part of the address space must be LOW (see Section 3.0, “Configurations” on page 13).

The number of address cycles required for each command varies. Refer to the command descriptions to determine addressing requirements. Addresses are typically ignored by die (LUNs) that are busy (RDY = 0); however, some addresses such as address cycles that follow the READ STATUS ENHANCED (78h) command, are accepted by die (LUNs), even when they are busy.

Figure 32. Synchronous ONFI 3.0 Addresses Cycle



7.10 Synchronous ONFI 3.0 Data Input

To enter the onfi 3.0 data input mode, the following conditions must be met:

- CE# is LOW
- ALE and CLE are LOW
- RE# is HIGH
- tWPRE is met
- DQS is LOW

Upon entering the onfi 3.0 data input mode after ^{t}WPRE, data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when CE# is LOW, RE# is HIGH, and ALE and CLE are LOW.

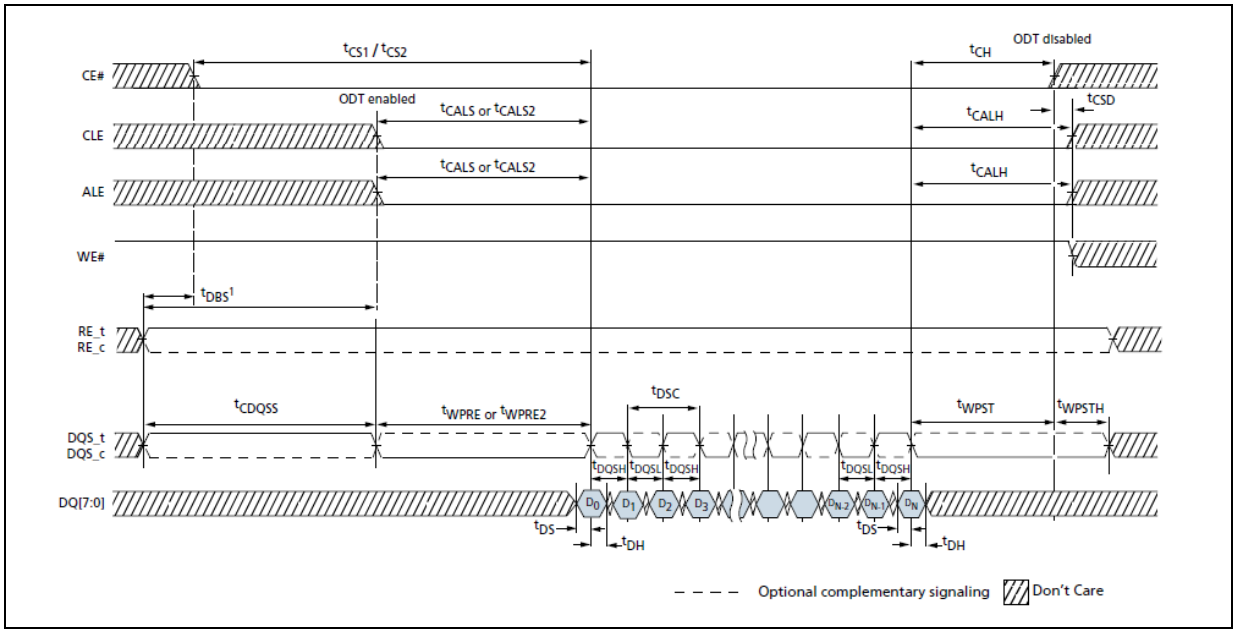
To exit onfi 3.0 data input mode, the following conditions must be met:

- CE# is LOW
- ALE and CLE are LOW
- RE# is HIGH
- The final two data bytes of the data input sequence are written to DQ[7:0] to the cache register on the rising and falling edges of DQS after the last cycle in the data input sequence
- DQS is held LOW for tWPST (after the final falling edge of DQS)

Following tWPST, the bus enters bus idle mode.

Data input is ignored by die (LUNs) that are not selected or are busy.

Figure 33. Synchronous ONFI 3.0 Data Input Cycles



Note: 1. ODT may not be required to be used for data input. If ODT is selected for use via SET FEATURES (EFh), then ODT is enabled and disabled during the points indicated.

7.11 Synchronous ONFI 3.0 Data Output

Data can be output from a die (LUN) if it is ready. Data output is supported following a READ operation from the NAND Flash array.

To enter the onfi 3.0 data output mode, the following conditions must be met:

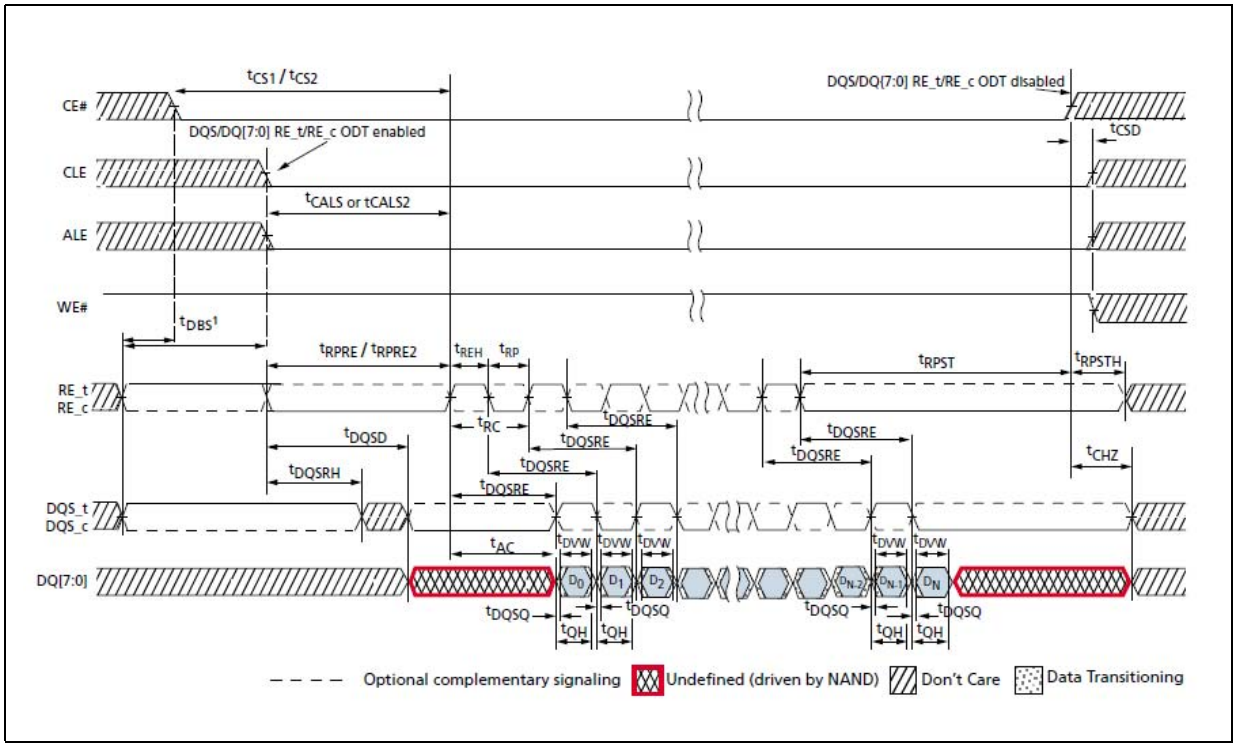
- CE# is LOW
- The host has released the DQ[7:0] bus and DQS
- ALE and CLE are LOW
- tRPRE is met

Upon entering the onfi 3.0 data output mode, DQS will toggle HIGH and LOW with a delay of ^{t}DQSRE from the respective rising and falling edges of RE#. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than ^{t}AC.

The final two data bytes are output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur ^{t}DQSRE after the last cycle in the data output sequence. The host must hold RE# for ^{t}RPST after the last RE# falling edge for data output.

Data output requests are typically ignored by a die (LUN) that is busy (RDY = 0); however, it is possible to output data from the status register even when a die (LUN) is busy by issuing the READ STATUS (70h) or READ STATUS ENHANCED (78h) command.

Figure 34. Synchronous ONFI 3.0 Data Output Cycles



Note: 1. ODT may not be required to be used for data output. If ODT is selected for use via SET FEATURES (EFh), then ODT is enabled and disabled during the points indicated.

7.12 Write Protect

See “Write Protect” in “Bus Operation — Asynchronous Interface” on page 17.

7.13 Ready/Busy#

See “Ready/Busy#” in “Bus Operation — Asynchronous Interface” on page 17.

8.0 Device Initialization

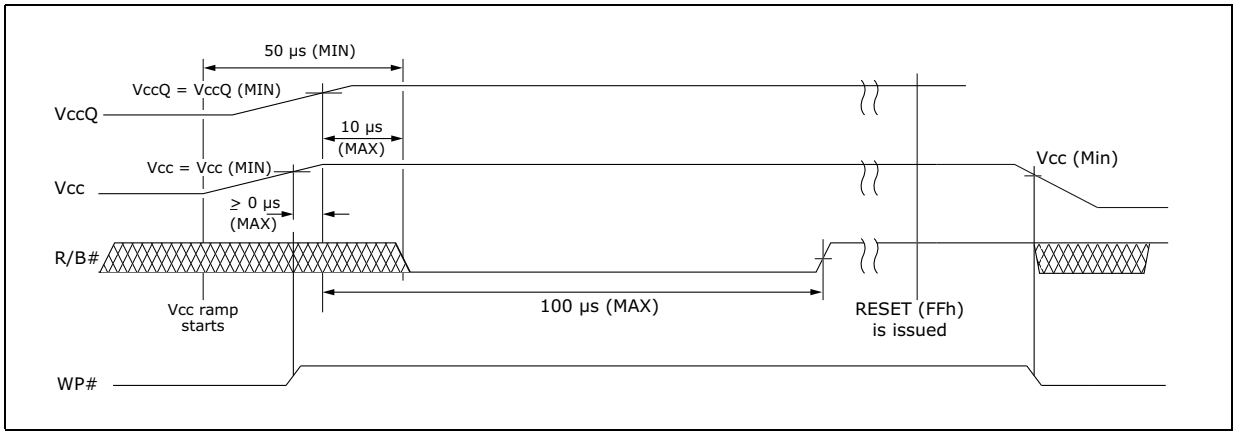
Intel NAND flash devices are designed to help prevent data corruption during power transitions. The WP#, CLE, and ALE signals should be kept at VIL during VCC ramp up or down to avoid an inadvertent command latch. The WP# signal permits additional hardware protection during power transitions and is always recommended to be used during a V_{CC} transition.

When ramping V_{CC} and V_{CCQ}, use the following procedure to initialize the device:

1. Set WP# signal to V_{IL}.
2. Ramp V_{CC} to 2.7-3.6 V.
3. Ramp V_{CCQ} to MIN-MAX no sooner than the V_{CC} ramp.
4. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target. The R/B# signal becomes valid when:
   - 50 µs has elapsed since the beginning of V_{CC} ramp, and
   - 10 µs has elapsed since V_{CC}/V_{CCQ} reached MIN
5. If not monitoring R/B#, the host must wait at least 100 µs after V_{CC}/V_{CCQ} reaches MIN.
6. All of the targets on the device power-on with the asynchronous interface active. Each NAND LUN draws less than an average of 10 mA (IST) measured over intervals of 1 ms until the RESET (FFh) command is issued.
7. The RESET (FFh) command must be issued to all targets (CE#s) as the first command after the NAND flash device is powered on. Each target will be busy for a maximum of 1 ms after the RESET command is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command to poll the status register.
8. The device is now initialized and ready for normal operations.

At power-down, V_{CCQ} must go LOW, either before, or simultaneously with, V_{CC} going LOW.

Figure 35. R/B# Power-On Behavior



Note:

1. If V_{CC} takes 40 µs or greater to reach V_{CC}_min from the start of the V_{CC} ramp, then R/B shall be valid 10 µs after reaching V_{CC}_min. If V_{CC} takes less than 40 µs to reach V_{CC}_min from the start of the V_{CC} ramp, then R/B shall be valid 50 µs from the start of the V_{CC} ramp.
2. When V_{CC} reaches Vss_min, R/B# will be valid HIGH within 100 µs. The host can then issue the RESET (FFh) command.

8.1 VPP Initialization

When ramping VPP, use the following procedure to initialize the VPP functionality:

1. VCC must be successfully ramped prior to the start of ramping VPP.
2. Ramp VPP.
3. VPP must be within its valid range prior to the SET FEATURES (EFh) command to enable the VPP functionality.

At power-down, VPP must go LOW to 0V before VCC going LOW.

9.0 Activating Interfaces

After performing the steps under “Device Initialization” on page 53, the asynchronous interface is active for all targets on the device.

Each target's interface is independent of other targets, so the host is responsible for changing the interface for each target.

If the host and NAND Flash device, through error, are no longer using the same interface, steps under Activating the Asynchronous Interface are performed to resynchronize the interfaces.

9.1 Activating the Asynchronous Interface

To activate the asynchronous NAND interface, once the synchronous interface is active, the following steps are repeated for each target:

1. The host pulls CE# HIGH, disables its input to CLK, and enables its asynchronous interface.
2. The host pulls CE# LOW and issues the RESET (FFh) command, using an asynchronous command cycle.
3. R/B# goes LOW for tRST.
4. After ^{t}ITC, and during ^{t}RST, the device enters the asynchronous NAND interface. READ STATUS (70h) and READ STATUS ENHANCED (78h) are the only commands that can be issued.
5. After ^{t}RST, R/B# goes HIGH. Timing mode feature address (01h), subfeature parameter P1 is set to 00h, indicating that the asynchronous NAND interface is active and that the device is set to timing mode 0.

For more details, see Section 12.0, “Reset Operations” on page 65.

9.2 Activating the Synchronous ONFI 2.3 Interface

To activate the synchronous ONFI 2.3 NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the Timing mode feature address.
3. Write P1 with 1Xh, where "X" is the timing mode used in the onfi 2.3 interface (see Configuration Operations).
4. Write P2–P4 as 00h-00h-00h.
5. R/B# goes LOW for ^{t}ITC. The host should pull CE# HIGH. During ^{t}ITC, the host should not issue any type of command, including status commands, to the NAND Flash device.
6. After ^{t}ITC, R/B# goes HIGH and the synchronous interface is enabled. Before pulling CE# LOW, the host should enable the clock.

9.3 Activating the Synchronous ONFI 3.0 Interface

Transitions from synchronous ONFI 2.3 directly to synchronous ONFI 3.0 (or vice versa) are not supported. In this case, the host should transition to the asynchronous interface and then select the desired synchronous interface

Prior to selecting the synchronous ONFI 3.0 interface, it is recommended that settings for the synchronous ONFI 3.0 interface be configured. Specifically:

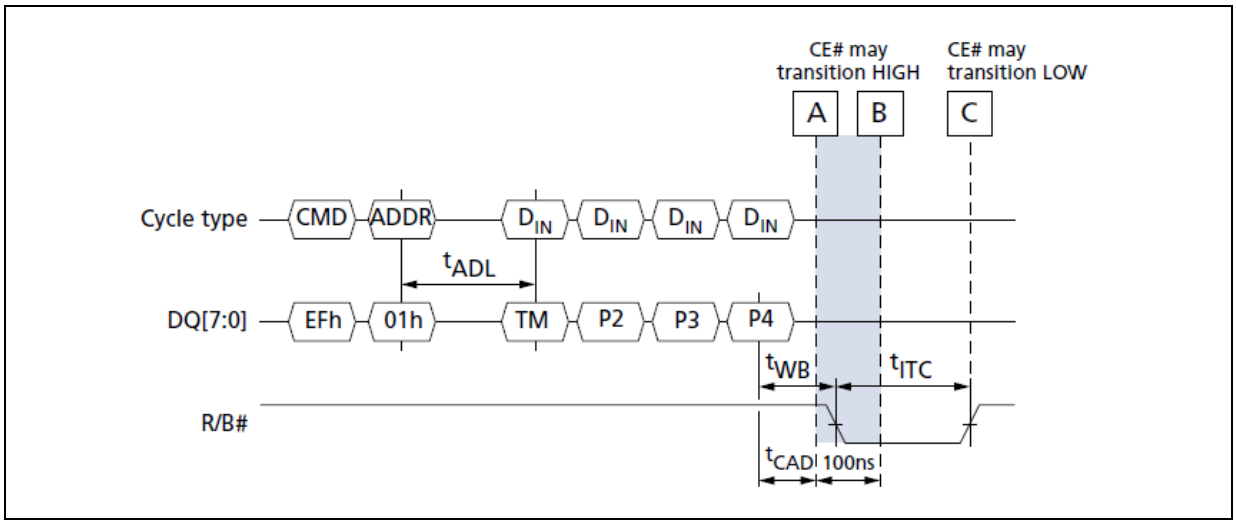
- SET FEATURES (EFh) command should be used to configure the onfi 3.0 Configuration feature address.
- If on-die termination (ODT) is used, the appropriate ODT CONFIGURE (E2) commands should be issued.

These actions should be completed prior to selecting the onfi 3.0 interface. If these settings are modified when the onfi 3.0 interface is already selected, the host should take care to ensure appropriate settings are applied in a manner that avoids signal integrity issues.

To activate the onfi 3.0 NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the Timing mode feature address.
3. Write P1 with 2Xh, where "X" is the timing mode used in the onfi 3.0 interface (see Section 14.0, “Configuration Operations” on page 73).
4. Write P2–P4 as 00h-00h-00h.
5. R/B# goes LOW for ^{t}ITC. The host should pull CE# HIGH. During ^{t}ITC, the host should not issue any type of command, including status commands, to the NAND Flash device.
6. After ^{t}ITC, R/B# goes HIGH and the onfi 3.0 interface is enabled.

Figure 36. Activating Interfaces



Note: 1. TM = Timing mode.

10.0 CE# Pin Reduction and Volume Addressing

In higher density capacity implementations there may be a significant number of CE# pins required for a host to support where there are many NAND packages with two to four CE# pins per package. The CE# pin reduction mechanism enables a single CE# pin from the host to be shared by multiple NAND Targets, thus enabling a significant reduction in the number of CE# pins required by the host system. The CE# pin reduction mechanism may be utilized with any data interface (asynchronous, onfi 2.3, onfi 3.0).

In the CE# pin reduction mechanism, each NAND package is appointed a Volume address during the initialization sequence. After initialization is complete, the host may address a particular Volume (i.e. NAND Target) by using the VOLUME SELECT (E1h) command. See VOLUME SELECT (E1h) for more details.

ENi and ENo pins are added to each NAND package and a daisy chain is created between NAND packages. The first NAND package in the chain has ENi not connected. All other NAND packages have their ENi pin connected to the previous package's ENo pin in a daisy chain configuration.

At power-on, the ENo pins are driven LOW by the NAND device. ENo shall be HiZ when all CE# signals on the NAND package are HIGH. When a NAND Target has had a Volume address appointed with the SET FEATURES (EFh) command, then the ENo pin shall be pulled HIGH by the NAND Target when the corresponding CE# is LOW. This enables the next NAND Target on a subsequent package in the daisy chain to accept commands since the ENi pin pulls HIGH when ENo is no longer pulling LOW. After a Volume address has been appointed to a Volume (i.e., NAND Target), that Volume shall become deselected and ignores the ENi pin until the next power cycle.

The state of ENi determines whether the NAND package is able to accept commands. If the ENi pin is HIGH and CE# is LOW for the NAND Target, then the NAND Target shall accept commands. If the ENi pin is LOW or CE# is HIGH for the NAND Target, then the NAND Target shall not accept commands.

To be selected to process a command, the Volume Select command shall be issued to the Host Target using the Volume address that was previously appointed for a particular NAND Target. After the CE# signal is pulled high for ^{t}CEH time, all LUNs on a Volume revert to their previous states.

Figure 37. CE# Pin Reduction Topology with single channel

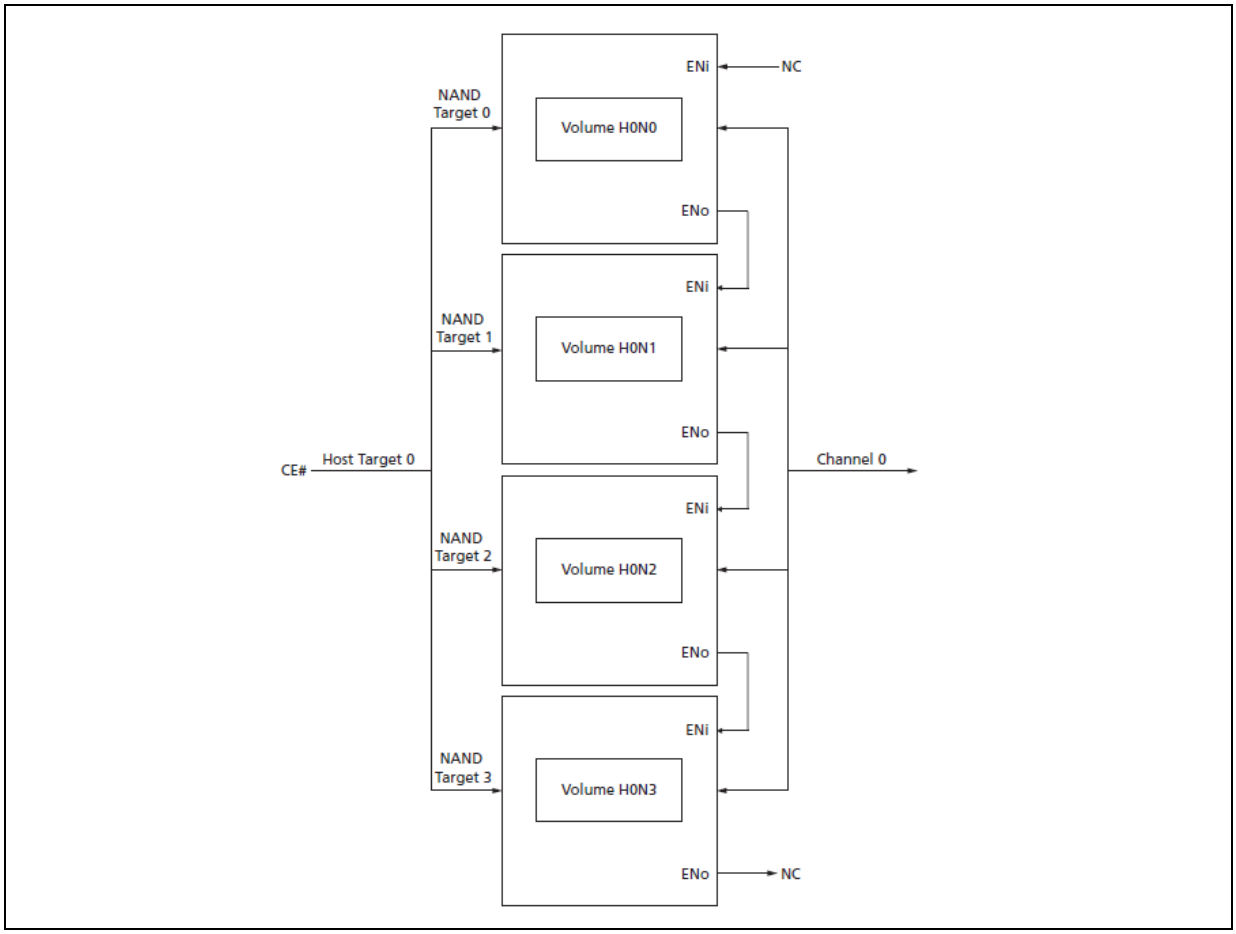
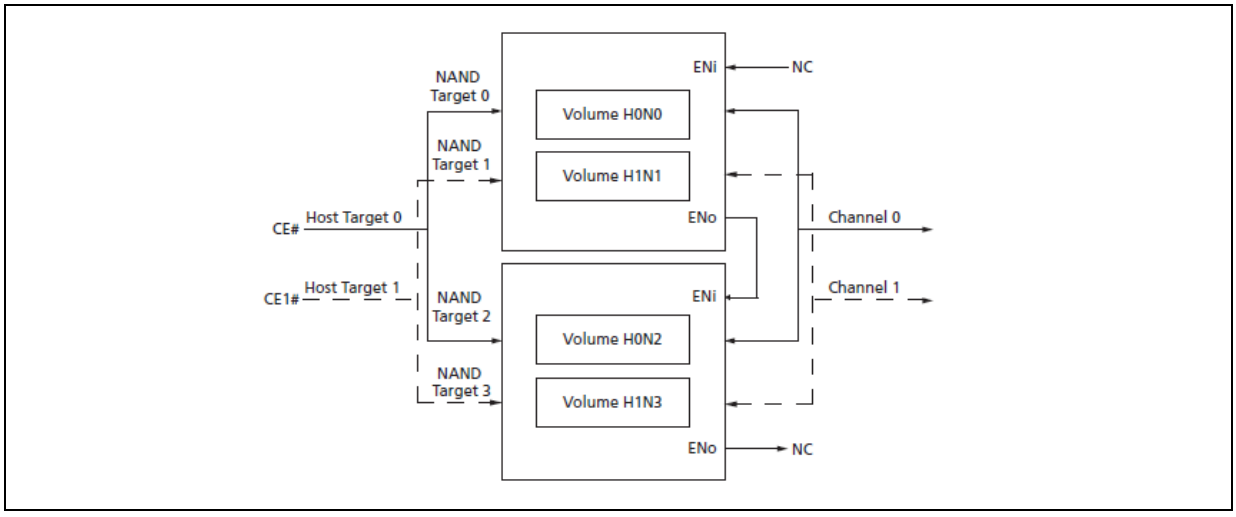


Figure 38. CE# Pin Reduction and Volume Addressing Topology with dual channel



10.1 Initialization Sequence

The host may issue a RESET (FFh) to all Targets in parallel on the selected Host Target, or the host may sequentially issue RESET (FFh) to each Target. The methodology chosen depends on host requirements for maximum current draw. To reset all Targets in parallel, the host issues a RESET (FFh) as the first command issued to the NAND device(s).

To reset Targets sequentially, the host issues a READ STATUS (70h) command as the first command issued to all NAND Targets on the selected Host Target.

During initialization when addressing a newly selected NAND Target with an initial command, the host shall wait for the ENo signal to be propagated to the ENi of the subsequent Target. Before addressing a new Target, the host shall wait (tENo + tENi) and should also include signal propagation time.

In cases where there are multiple NAND Targets within a package (for example, CE#s), those NAND Targets share the same ENo signal, the host shall not stagger SET FEATURES (EFh) commands that appoint the Volume addresses. If the SET FEATURES (EFh) commands are not issued simultaneously then the host shall wait until Volume appointment for previous NAND Target(s) is complete before issuing the next SET FEATURES (EFh) command to appoint the Volume address for the next NAND Target that shares the ENo within a package.

After issuing the SET FEATURE (EFh) command to appoint the Volume address, the host shall not issue another command to any NAND Target on the associated Host Target (including status commands) until after the tFEAT time has elapsed. This is to ensure that the proper NAND Target responds to the next command, allowing for the proper ENo/ENi signal levels to be reflected.

The initialization sequence when utilizing the CE# reduction functionality is as follows:

1. The host powers on the NAND device(s).
2. The host pulls CE# LOW.
3. If resetting all NAND Targets in parallel, then the host issues the RESET (FFh) command. This command is accepted by all NAND Targets connected to the CE# (Host Target).
4. If resetting each NAND Target sequentially, then:
   a. The host issues the READ STATUS (70h) command to check for ready status. Issuing the READ STATUS (70h) command prior to any other command indicates sequential RESET (FFh) of each NAND Target. The host then issues the RESET (FFh) command, which is only accepted by NAND devices with ENi set HIGH.
5. R/B# goes LOW for tRST and can be monitored by the host by issuing READ STATUS (70h) commands.
6. The host configures the NAND Target via commands necessary to perform that function (i.e. READ PARAMETER PAGE (ECh) command, SET FEATURES (EFh) command, etc).
7. The host issues SET FEATURES (EFh) command to the Volume Configuration feature address to appoint the Volume address for the NAND Target. The Volume Address specified shall be unique amongst all NAND Targets. After the SET FEATURE (EFh) command completes, ENo is set to one and the Volume is deselected until a VOLUME SELECT (E1h) command is issued that selects the Volume. The host shall not issue another command to a NAND Target connected to the associated Host Target until after tFEAT time has elapsed.
8. For each NAND Target connected to a Host Target, steps 4-7 are repeated for sequential initialization and steps 5-7 are repeated for parallel initialization.

9. When no further NAND Targets are found connected to the Host Target , then repeat steps 2-8 for the next Host Target (i.e., host CE# pin).
10. To complete the initialization process, a VOLUME SELECT (E1h) command is issued to select the next Volume that is going to execute a command.

After Volume addresses have been appointed to all NAND Targets, the host may complete any additional initialization tasks (e.g., configure on-die termination (ODT) for onfi 3.0 mode) and then proceed with normal operation. Prior to issuing a command to a Volume, the VOLUME SELECT (E1h) command shall be issued.

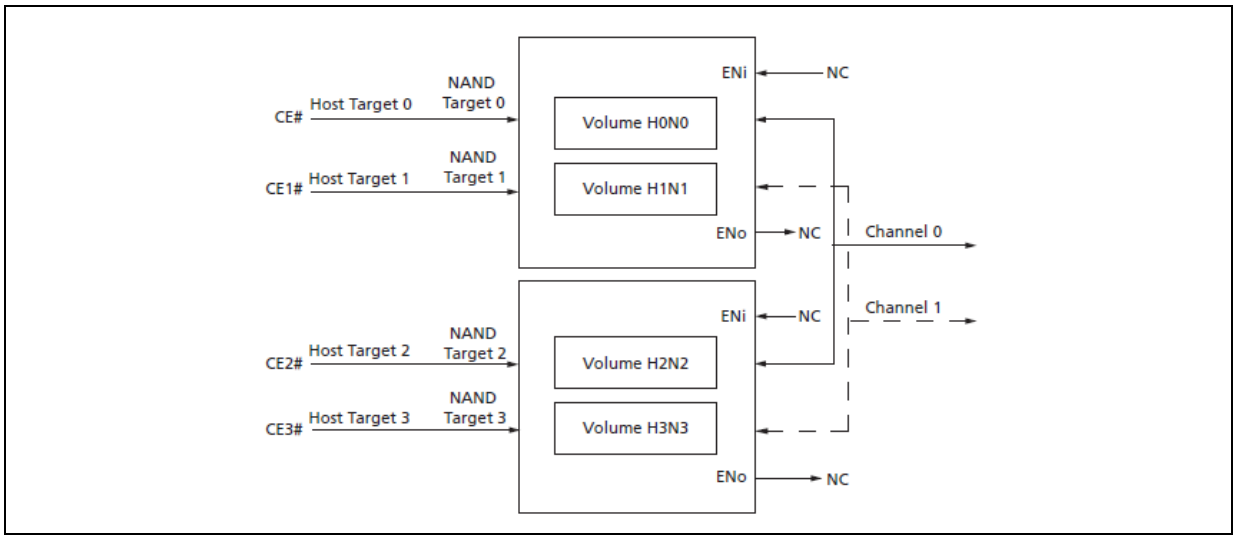
10.2 Volume Appointment without CE# Pin Reduction

If CE# pin reduction is not used (i.e. ENi and ENo are not connected) and the host desires to have the terminator on a package that does not share a CE# with the selected NAND Target, then each package that shares the CE# must have a Volume appointed at initialization using the SET FEATURE (EFh) command using the Volume Configuration feature.

Each CE# must have a unique Volume address appointed. Once all NAND Targets have Volume addresses appointed, the appointed Volume addresses may be used for termination selection. Volume addressing is not required for operation due to discrete CE# signals, however, the VOLUME SELECT (E1h) command is required for terminator selection when using non-Target termination schemes.

During operation, the CE# signal for the selected Volume and for any NAND Targets assigned as a terminator for the selected Volume need to be brought LOW. When CE# is brought LOW for an unselected Volume, all LUNs that are not assigned as terminators for the selected Volume are deselected.

Figure 39. Volume Addressing without CE# Pin Reduction Topology with dual channel



10.3 Appointing Volume Addresses

To appoint a Volume address, the Set Feature command is issued with a Feature Address of Volume Configuration. The Volume address is not retained across power cycles, and thus if Volume addressing is going to be used it needs to be appointed after each poweron prior to use of the NAND device(s).

10.4 Selecting a Volume

After Volume addresses have been appointed, every NAND Target (and associated LUN) is selected when the associated CE# is pulled LOW. The host issues a VOLUME SELECT (E1h) command to indicate the Volume (i.e. NAND Target) that shall execute the next command issued.

10.5 Multiple Volume Operation Restrictions

Volumes are independent entities. A multiple Volume operation is when two or more Volumes are simultaneously processing commands. Before issuing a command to an unselected Volume, CE# shall be pulled HIGH for a minimum of tCEH and the VOLUME SELECT (E1h) command shall then be issued to select the Volume to issue a command to next. While commands (including multi-LUN operations) are being performed on the selected Volume, a VOLUME SELECT (E1h) command is not required.

Issuing the same command to multiple Volumes at the same time is not supported. For a LUN level command (for example, READ, PROGRAM), the host may select a different Volume during a data input or data output operation and then resume the data transfer operation at a later time for a LUN level command. When re-selecting a Volume and associated LUN to complete the data input or data output operation, the following actions are required:

- Data input: The host shall issue a CHANGE ROW ADDRESS (85h) command prior to resuming data input.
- Data output: The host shall issue a CHANGE READ COLUMN ENHANCED (06h-E0h) or RANDOM DATA OUT (00h-05h-E0h) command prior to resuming data output.

For a Target level command (for example, GET FEATURES (EEh), SET FEATURES (EFh)), the host shall complete all data input or data output operations associated with that command prior to selecting a new Volume.

A Volume Select command shall not be issued during the following atomic portions of the COPYBACK, READ, PROGRAM, and ERASE operations:

- READ operations:
  - READ PAGE (00h-30h)
  - COPYBACK READ (00h-35h)
  - READ PAGE MULTI-PLANE (00h-32h)
  - READ PAGE CACHE RANDOM (00h-31h)
- PROGAM operations, note: The VOLUME SELECT (E1h) command may be issued prior to the 10h, 11h, or 15h command if the next command to this Volume is CHANGE ROW ADDRESS (85h):
  - PROGRAM PAGE (80h-10h)
  - PROGRAM PAGE MULTI-PLANE (80h/81h-11h)
  - PROGRAM PAGE CACHE (80h-15h)

- — COPYBACK PROGRAM (85h-10h)
- — COPYBACK PROGRAM MULTI-PLANE (85h-11h)

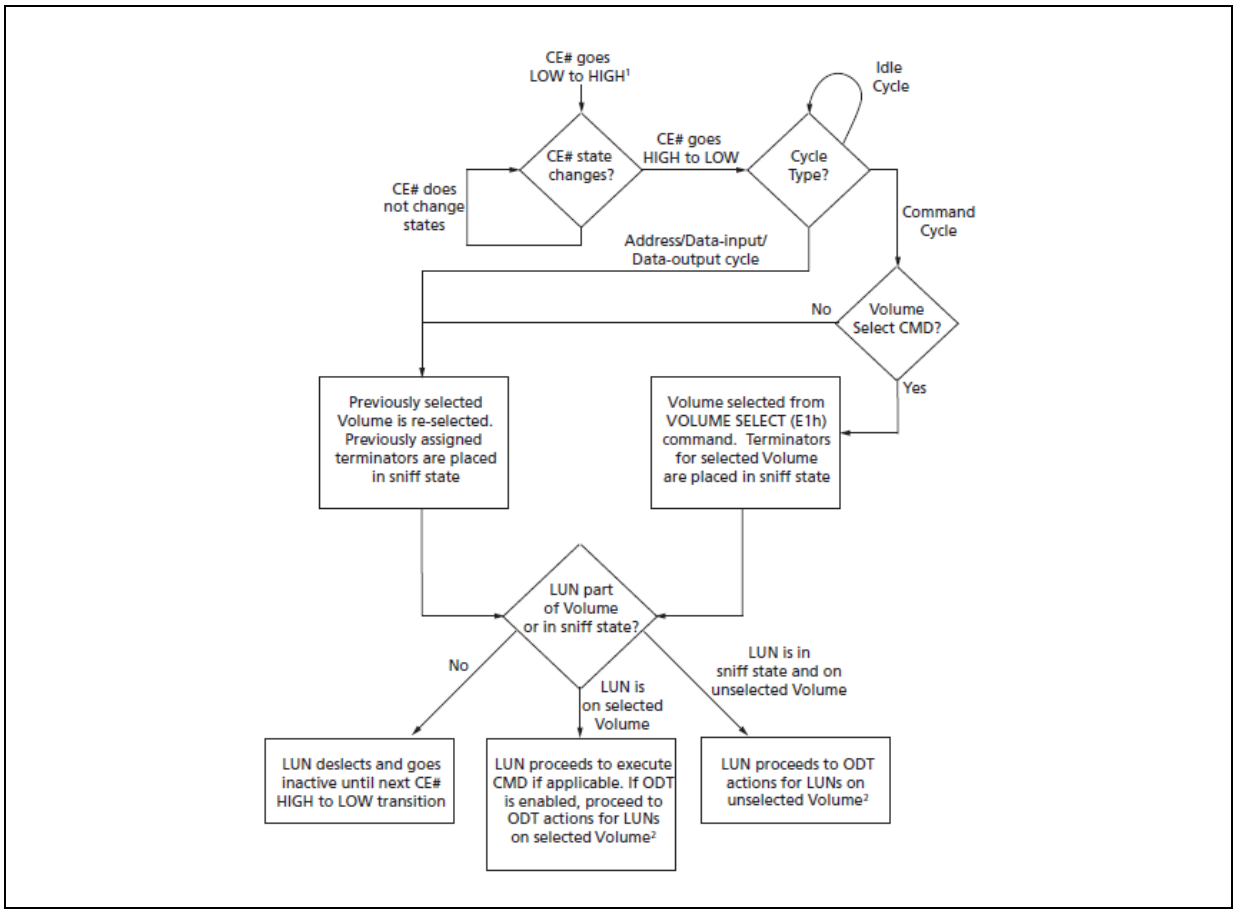
• ERASE operations:

- — ERASE BLOCK (60h-D0h)
- — ERASE BLOCK MULTI-PLANE (60h-D1h or 60h-60h-D0h)

10.6 Volume Reversion

When using Volume addressing, the LUNs shall support Volume reversion. Specifically, if CE# is transitioned from HIGH to LOW and a Volume Select is not the first command, then the LUN shall revert to the previously Selected, Sniff, and Deselected states based on the last specified Volume address. If on-die termination is enabled when using the onfi 3.0 data interface there are additional actions described within On Die Termination (ODT).

Figure 40. Volume Reversion behavioral flow



Notes:

1. This state is entered asynchronously when CE# transitions from LOW to HIGH.
2. ODT actions for LUNs on a selected Volume are specified in Figure 27 on page 41 .ODT actions for LUNs on an unselected Volume are specified in Figure 28 on page 42.

11.0 Command Definitions

Table 11. Command Set

Command	Command Cycle 1	Number of Address Cycles	Data Input Cycles	Command Cycle 2	Number of Valid Address Cycles 2	Command Cycle 3	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
Reset Command									
RESET	FFh	0	–	–	–	–	Yes	Yes	
SYNCHRONOUS RESET	FCh	0	–	–	–	–	Yes	Yes	
REST LUN	FAh	3	–	–	–	–	Yes	Yes	
Identification Commands									
READ ID	90h	1	–	–					3
READ PARAMETER PAGE	ECh	1	–	–					
READ UNIQUE ID	EDh	1	–	–					
Configuration Commands									
VOLUME SELECT	E1h	1	–						
ODT CONFIGURE	E2h	1	4						
SET FEATURES	EFh	1	4	–					4
GET FEATURES	EEh	1	–	–					3
Status Command									
READ STATUS	70h	0	–	–	–	–	Yes		
READ STATUS ENHANCED	78h	3	–	–	–	–	Yes	Yes	
Column Address Commands									
CHANGE READ COLUMN	05h	2	–	E0h				Yes	
CHANGE READ COLUMN ENHANCED (ONFI)	06h	5	–	E0h	–	–		Yes	
CHANGE READ COLUMN ENHANCED (JEDEC)	00H	5	–	05h	2	E0h		Yes	
CHANGE WRITE COLUMN	85h	2	Optional	–				Yes	
CHANGE ROW ADDRESS	85h	5	Optional	11h (optional)				Yes	5
Read Command									
READ MODE	00h	0	–	–	–	–		Yes	
READ PAGE	00h	5		30h	–	–		Yes	6
Read Cache Commands									
READ CACHE SEQUENTIAL	31h	–	–	–				Yes	4
READ CACHE RANDOM	00h	5	–	31h				Yes	4
READ CACHE END	3Fh	0	–	–				Yes	4

Table 11. Command Set (Continued)

Command	Command Cycle 1	Number of Address Cycles	Data Input Cycles	Command Cycle 2	Number of Valid Address Cycles 2	Command Cycle 3	Valid While Selected LUN is Busy[1]	Valid While Other LUNs are Busy[2]	Notes
Program Commands									
PAGE PROGRAM	80h	5	Yes	10h				Yes	
PAGE CACHE PROGRAM	80h	5	Yes	15h				Yes	5
Erase Command									
BLOCK ERASE	60h	3	–	D0h				Yes	
ERASE SUSPEND	61h	3	–	–	–	–	Yes	Yes	
ERASE RESUME	D2h	–	–	–	–	–		Yes	
Copyback Commands									
COPYBACK READ	00h	5	–	35h				Yes	
COPYBACK PROGRAM	85h	5	Optional	10h				Yes	

Notes:
1. Busy is RDY = 0. See Table 24, “Status Register (SR) Bit Definition” on page 82 for more information.
2. These commands may be used for Multi-LUN operations. See Section 21.0, “Multi-Plane Operations” on page 111 for more information.
3. The READ ID (90h) and GET FEATURES (EEh) output identical data on rising and falling DQS edges.
4. The SET FEATURES (EFh) command requires data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.
5. Command cycle #2 of 11h is conditional. See CHANGE ROW ADDRESS (85h) (page 118) for more details.
6. This command can be preceded by READ PAGE MULTI-PLANE (00h-32h) command to accommodate a maximum simultaneous multi-plane array operation.
7. Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE-series command; otherwise, it is prohibited.
8. Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise, it is prohibited.

Table 12. MULTI-PLANE Command Set

Command	Command Cycle 1	Number of Address Cycles	Command Cycle 2	Number of Address Cycles	Command Cycle 3	Valid During Busy	Notes
READ MULTI-PLANE	00h	5	32h-00h	5	30h	No	
SELECT CACHE REGISTER	06h	5	E0h	–	–	No	
READ STATUS ENHANCED	78h	3	–	–	–	Yes	2
PAGE PROGRAM MULTI-PLANE	80h	5	11h-80h	5	10h	No	2
PAGE CACHE PROGRAM MULTI-PLANE	80h	5	11h-80h	5	15h	No	2
COPYBACK READ MULTI-PLANE	00h	5	00h	5	35h	No	1
COPYBACK PROGRAM MULTI-PLANE	85h	5	11h-85h	5	10h	No	1, 2
ERASE BLOCK MULTI-PLANE	60h	3	D1h-60h	3	D0h	No	2

Notes:
1. Do not cross plane address boundaries when using COPYBACK READ MULTI-PLANE and COPYBACK PROGRAM MULTI-PLANE. See "Array Organization" on page 16 for plane address boundary definitions.
2. These commands are valid during busy when interleaved die operations are being performed.
3. Multi-plane read cache mode is supported. 00h-5addr(P0)-00h-5addr(P1)-31h and 00h-5addr(P0)-32h-00h-5addr(P1)-31h are acceptable.

12.0 Reset Operations

12.1 RESET (FFh)

The RESET (FFh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all die (LUNs), even when they are busy.

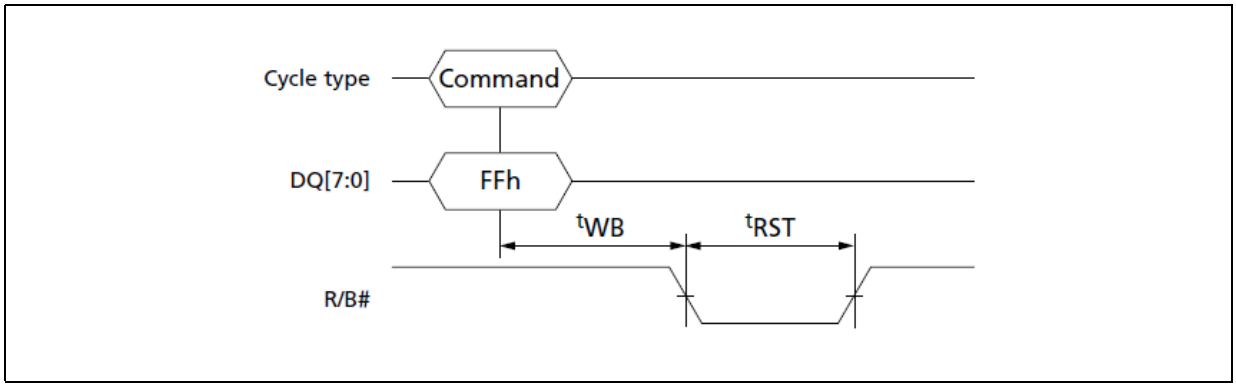
When FFh is written to the command register, the target goes busy for ^{t}RST. During ^{t}RST, the selected target (CE#) discontinues all array operations on all die (LUNs). All pending single- and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more die (LUNs), the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid.

RESET must be issued as the first command to each target following power-up. Use of the READ STATUS ENHANCED (78h) command is prohibited during the power-on RESET. To determine when the target is ready, use READ STATUS (70h).

If the RESET (FFh) command is issued when the synchronous interface is enabled, the target's interface is changed to the asynchronous interface and the timing mode is set to 0. The RESET (FFh) command can be issued asynchronously when the synchronous interface is active, meaning that CLK does not need to be continuously running when CE# is transitioned LOW and FFh is latched on the rising edge of CLK. After this command is latched, the host should not issue any commands during ^{t}ITC. After ^{t}ITC, and during or after ^{t}RST, the host can poll each LUN's status register.

If the RESET (FFh) command is issued when the asynchronous interface is active, the target's asynchronous timing mode remains unchanged. During or after ^{t}RST, the host can poll each LUN's status register.

Figure 41. RESET (FFh) Operation



12.2 SYNCHRONOUS RESET (FCh)

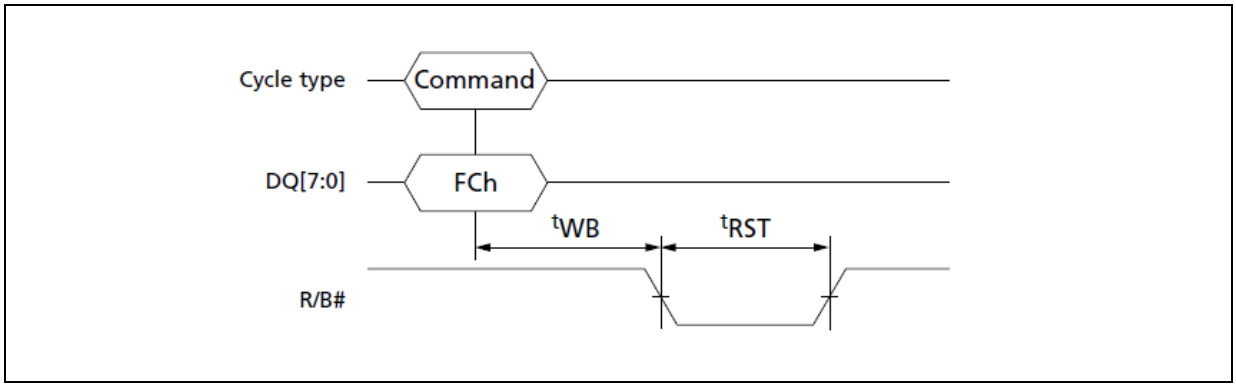
When the synchronous interface is active, the SYNCHRONOUS RESET (FCh) command is used to put a target into a known condition and to abort command sequences in progress.

This command is accepted by all die (LUNs), even when they are BUSY.

When FCh is written to the command register, the target goes busy for ^{t}RST. During ^{t}RST, the selected target (CE#) discontinues all array operations on all die (LUNs). All pending single- and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more die (LUNs), the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid and the synchronous interface remains active.

During or after ^{t}RST, the host can poll each LUN's status register. SYNCHRONOUS RESET is only accepted while the synchronous interface is active. Its use is prohibited when the asynchronous interface is active.

Figure 42. SYNCHRONOUS RESET (FCh) Operation



12.3 RESET LUN (FAh)

The RESET LUN (FAh) command is used to put a particular LUN on a target into a known condition and to abort command sequences in progress. This command is accepted by only the LUN addressed by the RESET LUN (FAh) command, even when that LUN is busy.

When FAh is written to the command register, the addressed LUN goes busy for ^{t}RST.

During ^{t}RST, the selected LUN discontinues all array operations. All pending single- and multi-plane operations are canceled. If this command is issued while a PROGRAM or ERASE operation is occurring on the addressed LUN, the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid.

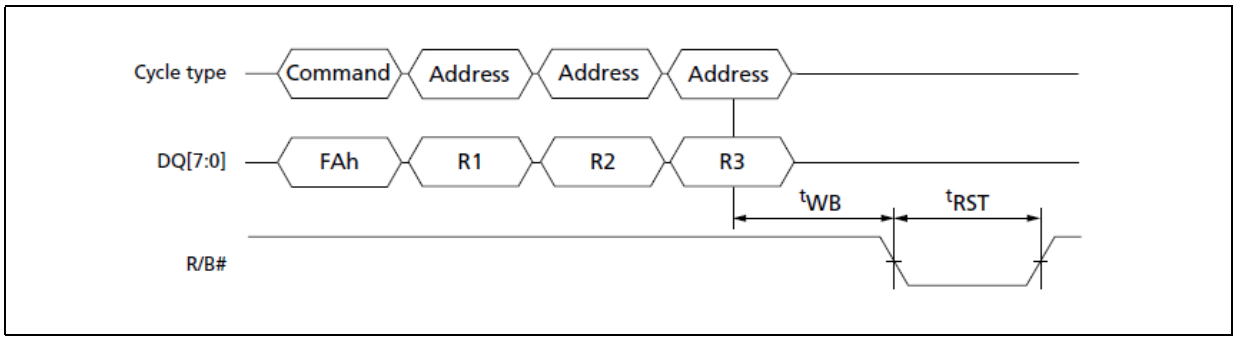
If the RESET LUN (FAh) command is issued when the synchronous interface is enabled, the targets's interface remains in synchronous mode.

If the RESET LUN (FAh) command is issued when the asynchronous interface is enabled, the target's interface remains in asynchronous mode.

During or after ^{t}RST, the host can poll each LUN's status register.

The RESET LUN (FAh) command is prohibited when not in the default array operation mode. The RESET LUN (FAh) command can only be issued to a target (CE#) after the RESET (FFh) command has been issued as the first command to a target following power-up.

Figure 43. RESET LUN (FAh) Operation



13.0 Identification Operations

13.1 READ ID (90h)

The READ ID (90h) command is used to read identifier codes programmed into the target.

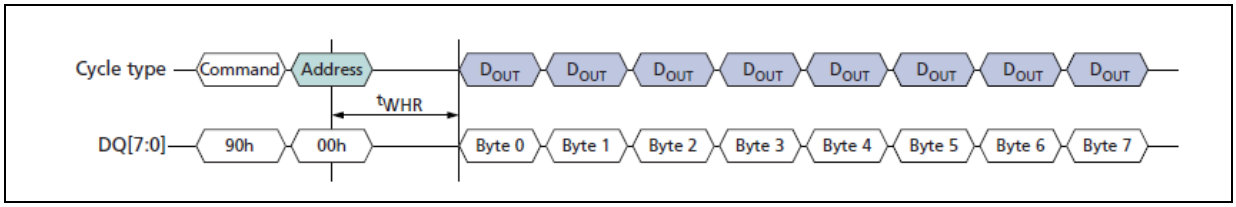
This command is accepted by the target only when all die (LUNs) on the target are idle. Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by a 00h address cycle, the target returns a 5-byte identifier code that includes the manufacturer ID, device configuration, and part-specific information.

When the 90h command is followed by a 20h address cycle, the target returns the 4-byte ONFI identifier code. When the 90h command is followed by a 40h address cycle, the target returns the 5-byte JEDEC identifier code.

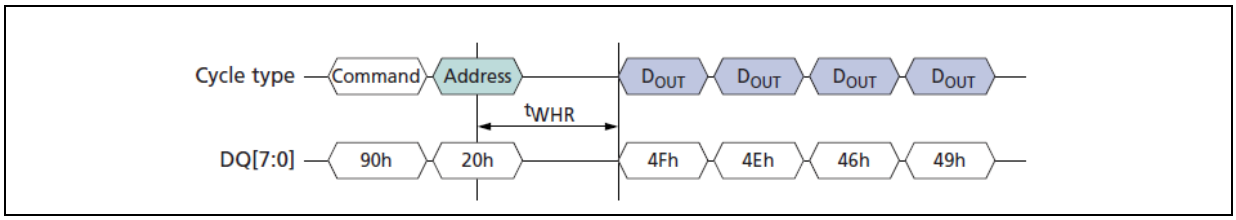
After the 90h and address cycle are written to the target, the host enables data output mode to read the identifier information. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, one data byte is output per rising edge of DQS when ALE and CLE are HIGH; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS.

Figure 44. READ ID (90h) with 00h Address Operation



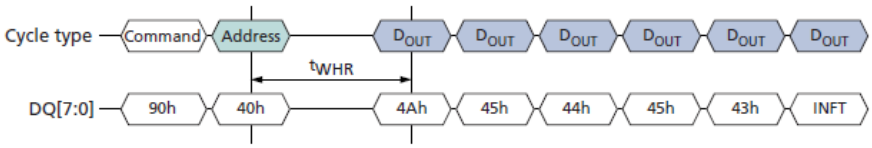
Notes: 1. See the READ ID Parameter tables for byte definitions.

Figure 45. READ ID (90h) with 20h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.

Figure 46. READ ID (90h) with 40h Address Operation



Note: 1. See the READ ID Parameter tables for byte definitions.

13.2 READ ID Parameter Tables

Table 13. Read ID Parameters for Address 00h

	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value
Byte 0	**Manufacturer ID**									
Manufacturer	Intel	1	0	0	0	1	0	0	1	
Byte value										89h
Byte 1	**Device ID**									
Vcc	3.3 V						1	0	0	100b
Density per CE#	64 Gb	0	1	1	0	0				01100b
Byte value		0	1	1	0		1	0	0	64h
Byte 2										
Number of LUNs per CE	1							0	0	00b
Cell type	MLC					0	1			01b
Pages per Block	512		1	1	0					110b
Multi-LUN operations	Not Supported	0								0b
Byte value		0	1	1	0	0	1	0	0	64h
Byte 3										
Page size	16 KB						1	0	0	100b
Spare area size per 512 B	37 B - 45 B		0	1	1	1				0111b
Reserved	Reserved	0								0b
Byte value		0	0	1	1	1	1	0	0	3Ch
Byte 4										
Planes per LUN	2							0	1	01b
Block per LUN	1024				0	0	0			000b
Async Timing mode	5 (20ns)	1	0	1						101b
Byte value		1	0	1	0	0	1	0	1	A1h
Byte 5										
Reserved[2]	Reserved	0	0	0	0					000b
Byte 6										
Reserved	Reserved	0	0	0	0	0	0	0	0	00h
Byte 7										
Reserved	Reserved	0	0	0	0	0	0	0	0	00h

Notes:
1. h = hexadecimal
2. Bits need to be fully programmable

Table 14. Read ID Parameters for Address 20h

Device	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
All	4Fh	4Eh	46h	49h	XXh

Notes:
1. h = hexadecimal
2. XXh = undefined

13.3 READ PARAMETER PAGE (ECh)

The READ PARAMETER PAGE (ECh) command is used to read the ONFI or JEDEC parameter page programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When the ECh command is followed by an 00h or 40h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

Use of the READ STATUS ENHANCED (78h) command is prohibited while the target is busy and during data output. After ^{t}R completes, the host enables data output mode to read the parameter page.

When the asynchronous interface is active, one data byte is output per RE# toggle.

When the synchronous interface is active, one data byte is output for each rising or falling edge of DQS.

A minimum of three copies of the parameter page are stored in the device. Each parameter page is 256 bytes. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the location of data output. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h or 00h-05h-E0h) command is prohibited.

The READ PARAMETER PAGE (ECh) output data can be used by the host to configure its internal settings to properly use the NAND Flash device. Parameter page data is static per part, however the value can be changed through the product cycle of NAND Flash. The host should interpret the data and configure itself accordingly.

Figure 47. READ PARAMETER (ECh) with 00h Address Operation for ONFI

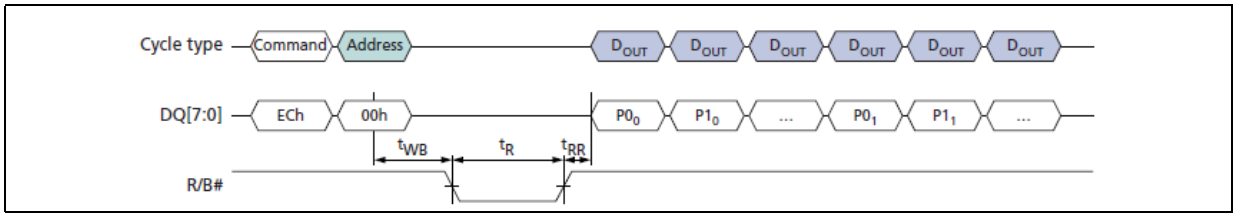
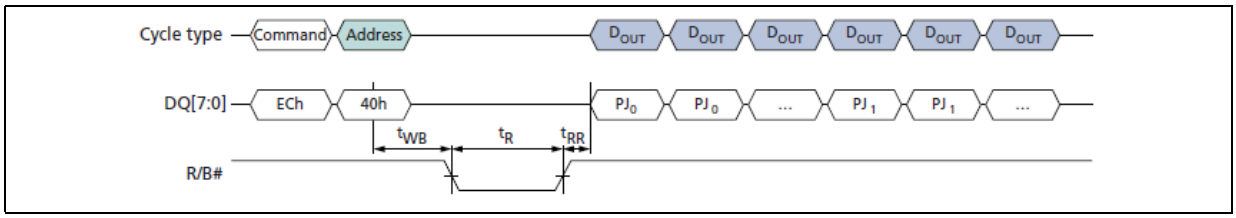


Figure 48. READ PARAMETER (ECh) with 40h Address Operation for JEDEC



Note: 1. h = hexadecimal

13.4 READ UNIQUE ID (EDh)

The READ UNIQUE ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when all die (LUNs) on the target are idle.

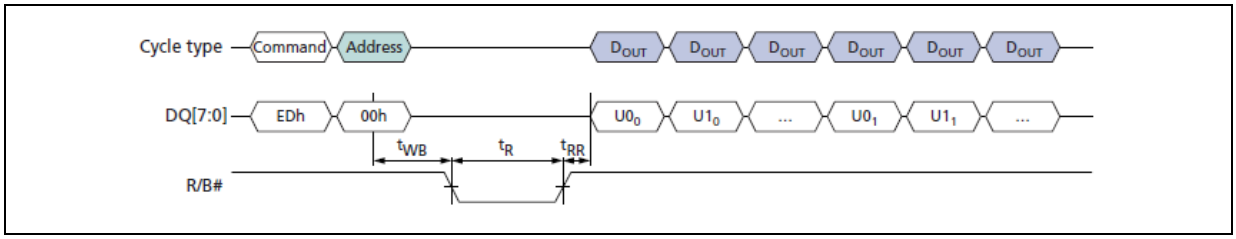
Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

When the EDh command is followed by a 00h address cycle, the target goes busy for tR. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

After tR completes, the host enables data output mode to read the unique ID. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, two data bytes are output, one byte for each rising or falling edge of DQS.

Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the data output location. Use of the CHANGE READ COLUMN ENHANCED (06h-E0h) command is prohibited.

Figure 49. READ UNIQUE ID (EDh) Operation



14.0 Configuration Operations

The SET FEATURES (EFh) and GET FEATURES (EEh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which subfeature parameters will be read or modified. The SET FEATURES (EFh) command writes subfeature parameters (P1-P4) to the specified feature address. The GET FEATURES (EEh) command reads the subfeature parameters (P1-P4) at the specified feature address.

Unless otherwise specified, the values of the feature addresses do not change when RESET (FAh, FFh, FCh) is issued by the host.

Table 15. Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h	onfi 3.0 configuration
03h–0Fh	Reserved
10h	Programmable output drive strength
11h–29h	Reserved
30h	VPP Configuration
31h-57h	Reserved
58h	Volume configuration
59h-79h	Reserved
80h	Programmable output drive strength
81h	Programmable RB# pull-down strength
83h–84h	Reserved
94h	R/B# configuration (see appendix)
96h–9Eh	Reserved
DBh-FFh	Reserved

14.1 SET FEATURES (EFh)

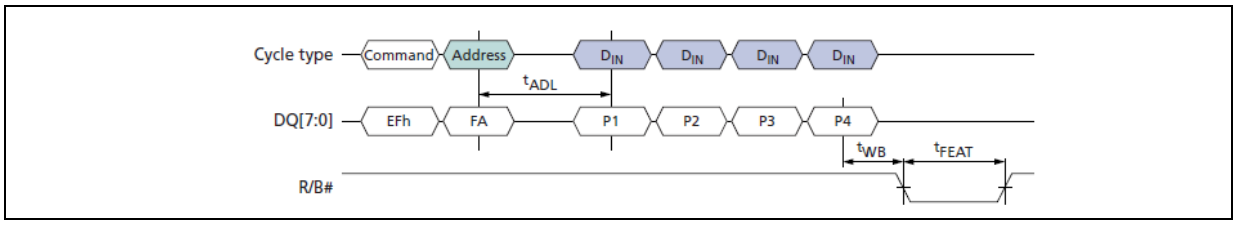
The SET FEATURES (EFh) command writes the subfeature parameters (P1-P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The EFh command is followed by a valid feature address as specified in . The host waits for ^{t}ADL before the subfeature parameters are input. When the asynchronous interface is active, one subfeature parameter is latched per rising edge of WE#. When the onfi 2.3 or onfi 3.0 interface is active, one subfeature parameter is latched per rising edge of DQS. The data on the falling edge of DQS should be identical to the subfeature parameter input on the previous rising edge of DQS. The device is not required to wait for the repeated data byte before beginning internal actions.

After all four subfeature parameters are input, the target goes busy for ^{t}FEAT. The READ STATUS (70h) command can be used to monitor for command completion. Feature address 01h (timing mode) operation is unique. If SET FEATURES is used to modify the interface type, the target will be busy for ^{t}ITC. See (page 0) for details.

Figure 50. SET FEATURES (EFh) Operation



14.2 GET FEATURES (EEh)

The GET FEATURES (EEh) command reads the subfeature parameters (P1-P4) from the specified feature address. This command is accepted by the target only when all die (LUNs) on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the EEh command is followed by a feature address, the target goes busy for tFEAT. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. During and prior to data output, use of the READ STATUS ENHANCED (78h) command is prohibited.

After ^{t}FEAT completes, the host enables data output mode to read the subfeature parameters. When the asynchronous interface is active, one data byte is output per RE# toggle. When the onfi 2.3 or onfi 3.0 interface is active, one subfeature parameter is output per DQS toggle on rising or falling edge of DQS.

Figure 51. GET FEATURES (EEh) Operation

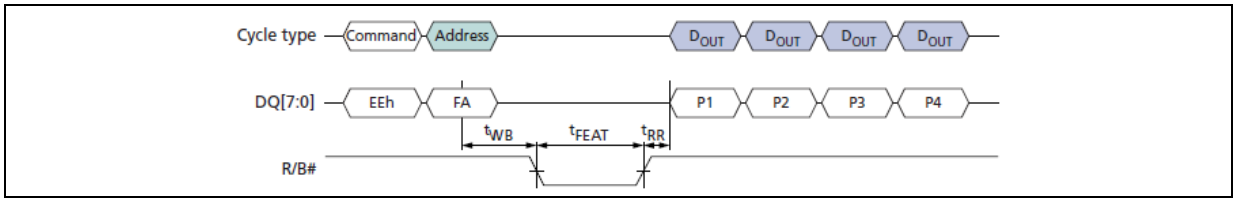


Table 16. Feature Address Timing Mode

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Timing mode	Mode 0 (default)					0	0	0	0	x0h	1,2
	Mode 1					0	0	0	1	x1h	
	Mode 2					0	0	1	0	x2h	
	Mode 3					0	0	1	1	x3h	
	Mode 4					0	1	0	0	x4h	
	Mode 5					0	1	0	1	x5h	
	Mode 6					0	1	1	0	x6h	
	Mode 7					0	1	1	1	x7h	
	Reserved					1	x	x	x	-	
Data Interface	Asynchronous (default)			0	0					0xh	1
	Synchronous ONFI 2.3			0	1					1xh	
	Onfi 3.0			1	0					2xh	
	Reserved			1	1					3xh	
Program clear	Program command clears all cache registers on target (default)			0						0b	
	Program command clears only addressed LUN cache register on a target		1							1b	
Reserved		0								0b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:

1. Asynchronous timing mode 0 is the default, power-on value.
2. If the onfi 2.3 or onfi 3.0 interface is active, a RESET (FFh) command will change the timing mode and data interface bits of feature address 01h to their default values. If the asynchronous interface is active, a RESET (FFh) command will not change the values of the timing mode or data interface bits to their default valued. Transition from the onfi 2.3 interface to the onfi 3.0 interface or vice versa is not permitted.

Table 17. Feature Address 02h: Onfi 3.0 Configuration

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Voltage Reference (VEN)	External VREFQ is disabled and internal voltage is used as reference for input and DQ signals (default)								0	0b	1,2
	External VREFQ is enabled and used as reference for input and DQ signals								1	1b	
Data Interface	Asynchronous (default)			0	0					0xh	1
	Synchronous ONFI 2.3			0	1					1xh	
	Onfi 3.0			1	0					2xh	
	Reserved			1	1					3xh	
Program clear	Program command clears all cache registers on target (default)			0						0b	
	Program command clears only addressed LUN cache register on a target		1							1b	
Reserved		0								0b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes:

1. If set to one, then external VREFQ is used as a reference for the input and I/O signals. If cleared to zero, then internal VREFQ is used as a reference for the input and I/O signals. This setting applies to input and I/O signals, including DQ[7:0], DQS_t, DQS_c, RE_t, RE_c,WE#, ALE, and CLE. CE# and WP# are CMOS signals and always use internal VREFQ.
2. If the onfi 3.0 interface is active, a RESET (FFh) command will change the timing mode and data interface bits of feature address 02h to their default values.
3. This field controls the on-die termination settings for the DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c signals. RTT settings may be specified separately for DQ[7:0]/DQS and the RE# signals. The DQ[7:0]/DQS may be specified separately for data input versus data output operation. Refer to the definition of the ODT CONFIGURE (E2h) command. If values are specified with the ODT CONFIGURE (E2h) command, then this field is not used. GET FEATURES (EEh) returns the previous value set in this field, regardless of the RTT settings specified using ODT CONFIGURE (E2h). If values are specified with the ODT Configure command, then this field is not used. Get Features returns the previous value set in this field, regardless of the RTT settings specified using ODT Configure.
4. Number of warmup cycles for and RE_t/RE_c and DQS_t/DQS_c for data output. The number of initial "dummy" RE_t/RE_c cycles at the start of data output operations for the . There are corresponding "dummy" DQS_t/DQS_c cycles to the "dummy" RE_t/RE_c cycles that the host shall ignore during data output.

5. This field indicates the number of warmup cycles of DQS that are provided for data input. These are the number of initial "dummy" DQS_t/DQS_c cycles at the start of data input operations.

Table 18. Feature Address 10h and 80h: Programmable Output Drive Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Output drive strength	18 Ohms							0	0	00h	1
	25 Ohms							0	1	01h	
	35 Ohms (default)							1	0	02h	
	50 Ohms							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. See Section 24.0, "Output Drive Impedance" on page 114 for details.

Table 19. Feature Address 30h: V_{PP}

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
External V_{PP} configuration	Disabled (default)								0	00h	1
	Enabled								1	01h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. This setting controls whether external VPP is enabled. This setting is retained across RESET (FAh, FCh, FFh) commands.

Table 20. Feature Address 58h: Volume configuration

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
Volume Address	Field used to assign a value for a given Volume Address					X	X	X	X		1
Reserved		0	0	0	0					0h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. After the Volume Address is appointed, the ENo pin for that Volume is set to one, the ENi pin for that Volume is ignored until the next power cycle, and the Volume is deselected until a VOLUME SELECT (E1h) command is issued that selects the associated Volume. The host shall only set this feature once per power cycle for each Volume. The address specified is then used in VOLUME SELECT (E1h) command for accessing this NAND Target. This setting is retained across RESET (FAh, FCh, FFh) commands.

Table 21. Feature Address 81h: Programmable R/B# Pull-Down Strength

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
P1											
R/B# pull-down strength	Full (defaul)							0	0	00h	1
	Three-quarter							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Note: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

14.3 VOLUME SELECT (E1h)

The Volume Select function is used to select a particular Volume based on the address specified. VOLUME SELECT (E1h) command is required to be used when CE# pin reduction is used or when matrix termination is used.

This command is accepted by all Targets that share a particular CE# pin. The command may be executed with any LUN on the Volume in any state. The VOLUME SELECT (E1h) command may only be issued as the first command after CE# is pulled LOW; CE# shall have remained HIGH for tCEH in order for the VOLUME SELECT (E1h) command to be properly received by all Targets on the Volume.

When the VOLUME SELECT (E1h) command is issued, all Targets that have a Volume address that does not match the address specified shall be deselected to save power (equivalent behavior to CE# pulled HGH). If one of the LUNs in an unselected Volume is the assigned terminator for the Volume addressed, then that LUN will enter the sniff state.

If the Volume address specified does not correspond to any appointed Volume address, then all Targets shall be deselected until a subsequent VOLUME SELECT (E1h) command is issued. If the VOLUME SELECT (E1h) command is not the first command issued after CE# is pulled LOW, then the Targets revert to their previous selected, deselected, or sniff states.

The Volume address is retained across all RESET (FAh, FCh, FFh) commands.

Figure 52. VOLUME SELECT (E1h) Operation

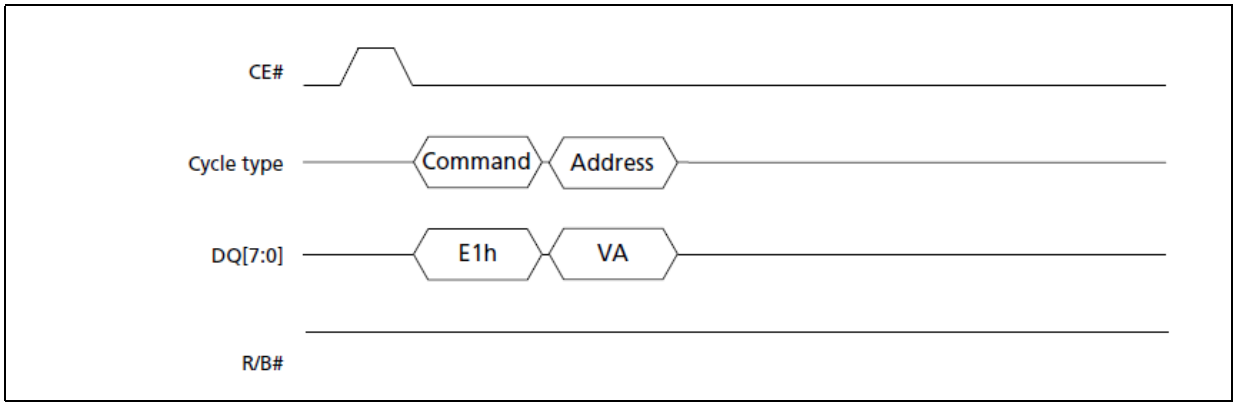


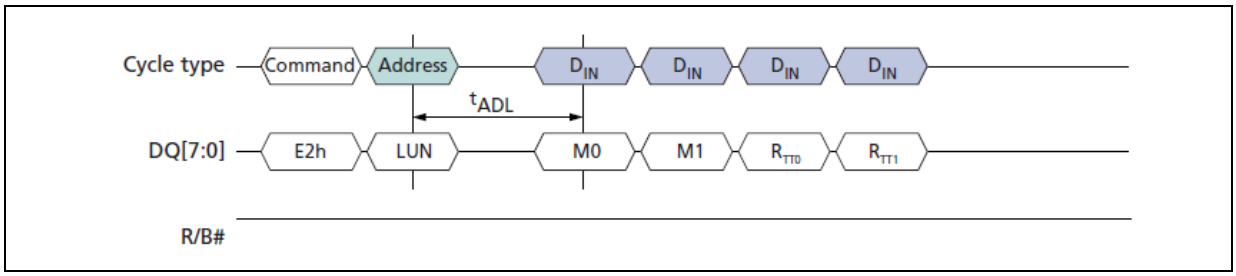
Table 22. Volume Address

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
Volume Address											
VA						Volume Address				-	
Reserved		0	0	0	0					-	

14.4 ODT CONFIGURE (E2h)

The ODT CONFIGURE (E2h) command is used to configure on-die termination. Specifically, ODT CONFIGURE (E2h) specifies whether a particular LUN is a terminator for a Volume(s) and the RTT settings. If the LUN is specified as a terminator for one or more Volumes, then the LUN shall enable on-die termination when either data input or data output cycles are executed on the Volume(s) it is acting as a terminator for depending on the settings of Table 23. The on-die termination settings are retained across all RESET (FAh, FCh, FFh) commands.

Figure 53. ODT CONFIGURE (E2h) Operation



The LUN address correspond to the same structure as the last address cycle for the NAND device which determines which LUN will act as the terminator.

The ODT Configuration Matrix structure is defined in Table 23. For the Volume Address fields M0 and M1, if a bit is set to one then the LUN shall act as the terminator for the corresponding Volume(s) (Vn) where n corresponds to the Volume address.

The ODT CONFIGURE (E2h) command is only available while in the onfi 3.0 interface operation mode.

Table 23. ODT Configuration Matrix

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
M0											
Volume Address	Volumes that will be terminated by selected LUN	V7	V6	V5	V4	V3	V2	V1	V0	-	
M1											
Volume Address	Volumes that will be terminated by selected LUN	V15	V14	V13	V12	V11	V10	V9	V8	-	
R_{TT0}											

Table 23. ODT Configuration Matrix (Continued)

Subfeature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value	Notes
DQ[7:0]/ DQS_t/ DQS_c RTT and ODT enable for data input	ODT disabled (default)					0	0	0	0	0h	
	ODT enabled with R_{TT} of 150 Ohms					0	0	0	1	1h	
	ODT enabled with R_{TT} of 100 Ohms					0	0	1	0	2h	
	ODT enabled with R_{TT} of 75 Ohms					0	1	0	0	4h	
	ODT enabled with R_{TT} of 50 Ohms					0	1	0	0	4h	
	Reserved					0	1	0	1	5h	
						0	1	1	1	6h	
						0	1	1	1	7h	
						1	X	X	X	8h-Fh	
DQ[7:0]/ DQS_t/ DQS_c RTT and ODT enable for data output	ODT disabled (default)	0	0	0	0					0h	
	ODT enabled with R_{TT} of 150 Ohms	0	0	0	1					1h	
	ODT enabled with R_{TT} of 100 Ohms	0	0	1	0					2h	
	ODT enabled with R_{TT} of 75 Ohms	0	0	1	1					3h	
	ODT enabled with R_{TT} of 50 Ohms	0	1	0	0					4h	
	Reserved	0	1	0	1					5h	
		0	1	1	0					6h	
		0	1	1	1					7h	
		1	X	X	X					8h-Fh	
R_{TT1}											
RE_t and RE_c RTT ODT enable	ODT disabled (default)					0	0	0	0	0h	
	ODT enabled with R_{TT} of 150 Ohms					0	0	0	1	1h	
	ODT enabled with R_{TT} of 100 Ohms					0	0	1	0	2h	
	ODT enabled with R_{TT} of 75 Ohms					0	0	1	1	3h	
	ODT enabled with R_{TT} of 50 Ohms					0	1	0	0	4h	
Reserved	-					0	1	0	1	5h	
						0	1	1	0	6h	
						0	1	1	1	7h	
						1	X	X	X	8h-Fh	
Reserved	-	0	0	0	0					0h	

15.0 Status Operations

Each die (LUN) provides its status independently of other die (LUNs) on the same target through its 8-bit status register.

After the READ STATUS (70h) or READ STATUS ENHANCED (78h) command is issued, status register output is enabled. The contents of the status register are returned on DQ[7:0] for each data output request.

When the asynchronous interface is active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

When the synchronous interface is active and status register output is enabled, changes in the status register are seen on DQ[7:0] as long as CE# and W/R# are LOW and ALE and CLE are HIGH. DQS also toggles while ALE and CLE are HIGH.

While monitoring the status register to determine when a data transfer from the Flash array to the data register (tR) is complete, the host must issue the READ MODE (00h) command to disable the status register and enable data output (see "READ MODE (00h)" on page 91).

The READ STATUS (70h) command returns the status of the most recently selected die (LUN). To prevent data contention during or following an interleaved die (multi-LUN) operation, the host must enable only one die (LUN) for status output by using the READ STATUS ENHANCED (78h) command (see Section 22.0, "Interleaved Die (Multi-LUN) Operations" on page 112).

Table 24. Status Register (SR) Bit Definition

SR Bit	Definition	Independent per Plane[1]	Definition
7	WP#	–	Write Protect 0 = Protected 1 = Not protected In the normal array mode, this bit indicates the value of the WP# signal. In OTP mode this bit is set to 0 if a PROGRAM OTP PAGE operation is attempted and the OTP area is protected.
6	RDY	–	Ready/Busy I/O 0 = Busy 1 = Ready This bit indicates that the selected die (LUN) is not available to accept new commands, address, or data I/O cycles with the exception of RESET LUN (FAh), SYNCHRONOUS RESET (FCh), RESET (FFh), READ STATUS (70h), and READ STATUS ENHANCED (78h). This bit applies only to the selected die (LUN).
5	ARDY	–	Ready/Busy Array 0 = Busy 1 = Ready This bit goes LOW (busy) when an array operation is occurring on any plane of the selected die (LUN). It goes HIGH when all array operations on the selected die (LUN) finish. This bit applies only to the selected die (LUN).
4	–	–	Reserved (0)
3	–	–	Reserved (0)
2	SUSPEND	–	Erase Suspend: Used in conjunction with FAIL of the status register (SR[0]) SUSPEND = 0, FAIL = 0: Erase operation completed with successful status. SUSPEND = 0, FAIL = 1: Erase operation completed with fail status. SUSPEND = 1, FAIL = 0: Erase operation successful suspended SUSPEND = 1, FAIL = 1: Reserved.

Table 24. Status Register (SR) Bit Definition

SR Bit	Definition	Independent per Plane[1]	Definition
1	FAILC	Yes	Pass/Fail (N) 0 = Pass 1 = Fail This bit is set if the previous operation on the selected die (LUN) failed. This bit is valid only when RDY (SR bit 6) is 1. It applies to PROGRAM-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 85h-10h). This bit is not valid following an ERASE-series or READ-series operation.
0	FAIL	Yes	Pass/Fail (N) 0 = Pass 1 = Fail This bit is set if the most recently finished operation on the selected die (LUN) failed. This bit is valid only when ARDY (SR bit 5) is 1. It applies to PROGRAM-, ERASE-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 60h-D0h, 85h-10h). This bit is not valid following a READ-series operation.

Note: 1. After a multi-plane operation begins, the FAILC and FAIL bits are ORed together for the active planes when the READ STATUS (70h) command is issued. After the READ STATUS ENHANCED (78h) command is issued, the FAILC and FAIL bits reflect the status of the plane selected.

15.1 READ STATUS (70h)

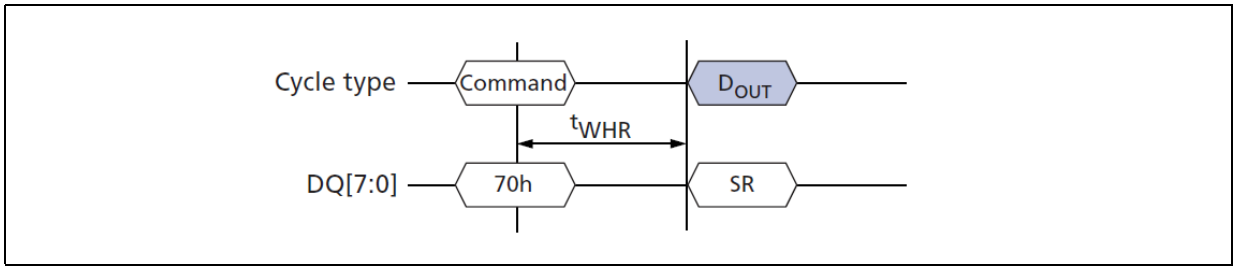
The READ STATUS (70h) command returns the status of the last-selected die (LUN) on a target. This command is accepted by the last-selected die (LUN) even when it is busy (RDY = 0).

If there is only one die (LUN) per target, the READ STATUS (70h) command can be used to return status following any NAND command.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select the die (LUN) that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as two or more die (LUNs) could respond until the next operation is issued. The READ STATUS (70h) command can be used following all single die (LUN) operations.

If following a multi-plane operation, regardless of the number of LUNs per target, the READ STATUS (70h) command indicates an error occurred (FAIL = 1), use the READ STATUS ENHANCED (78h) command—once for each plane—to determine which plane operation failed.

Figure 54. READ STATUS (70h) Operation



15.2 READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed die (LUN) on a target even when it is busy (RDY = 0). This command is accepted by all die (LUNs), even when they are BUSY (RDY = 0).

Writing 78h to the command register, followed by three row address cycles containing the page, block, and LUN addresses, puts the selected die (LUN) into read status mode.

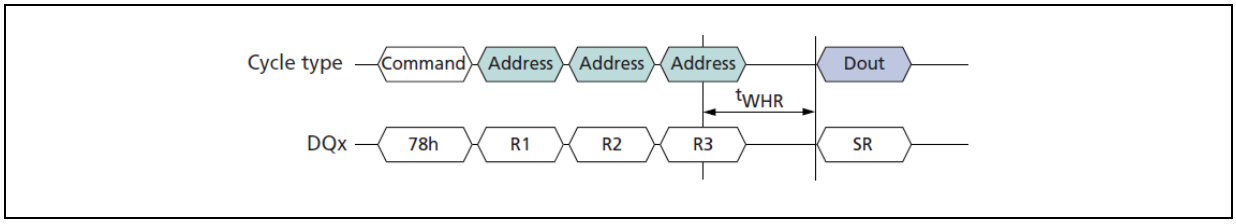
The selected die (LUN) stays in this mode until another valid command is issued. Die (LUNs) that are not addressed are deselected to avoid bus contention.

The selected LUN's status is returned when the host requests data output. The RDY and ARDY bits of the status register are shared for all of the planes of the selected die (LUN).

The FAILC and FAIL bits are specific to the plane specified in the row address. The READ STATUS ENHANCED (78h) command also enables the selected die (LUN) for data output. To begin data output following a READ-series operation after the selected die (LUN) is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command after the die (LUN) is ready (see “CHANGE READ COLUMN ENHANCED (06h-E0h)” on page 86).

Use of the READ STATUS ENHANCED (78h) command is prohibited during the poweron RESET (FFh) command and when OTP mode is enabled. It is also prohibited following some of the other reset, identification, and configuration operations. See individual operations for specific details.

Figure 55. READ STATUS ENHANCED (78h) Operation



16.0 Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the selected die (LUNs). These features provide host flexibility for managing data, especially when the host internal buffer is smaller than the number of data bytes or words in the cache register.

When the asynchronous interface is active, column address operations can address any byte in the selected cache register.

When the synchronous interface is active, column address operations are aligned to word boundaries (CA0 is forced to 0), because as data is transferred on DQ[7:0] in two-byte units.

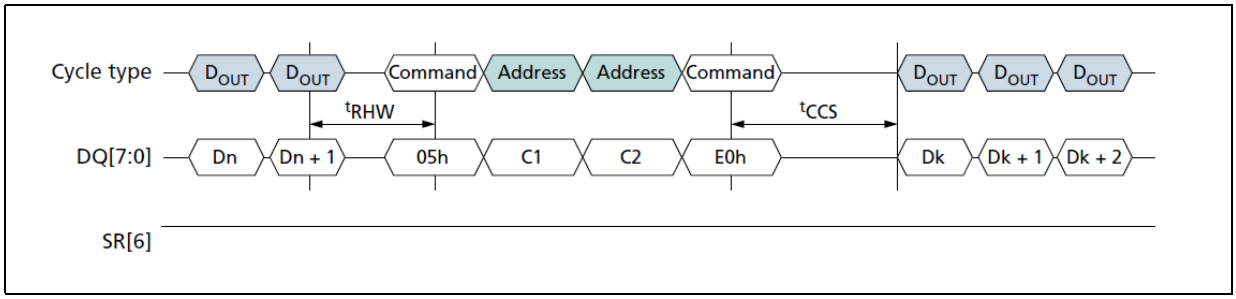
16.1 CHANGE READ COLUMN (05h-E0h)

The CHANGE READ COLUMN (05h-E0h) command changes the column address of the selected cache register and enables data output from the last selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during CACHE READ operations (RDY = 1; ARDY = 0).

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the selected die (LUN) into data output mode. After the E0h command cycle is issued, the host must wait at least ^{t}CCS before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be issued prior to issuing the CHANGE READ COLUMN (05h-E0h). In this situation, using the CHANGE READ COLUMN (05h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

Figure 56. CHANGE READ COLUMN (05h-E0h) Operation



16.2 CHANGE READ COLUMN ENHANCED (06h-E0h)

The CHANGE READ COLUMN ENHANCED (06h-E0h) command enables data output on the addressed die's (LUN's) cache register at the specified column address. This command is accepted by a die (LUN) when it is ready (RDY = 1; ARDY = 1).

Writing 06h to the command register, followed by two column address cycles and three row address cycles, followed by E0h, enables data output mode on the address LUN's cache register at the specified column address. After the E0h command cycle is issued, the host must wait at least tCCS before requesting data output. The selected die (LUN) stays in data output mode until another valid command is issued.

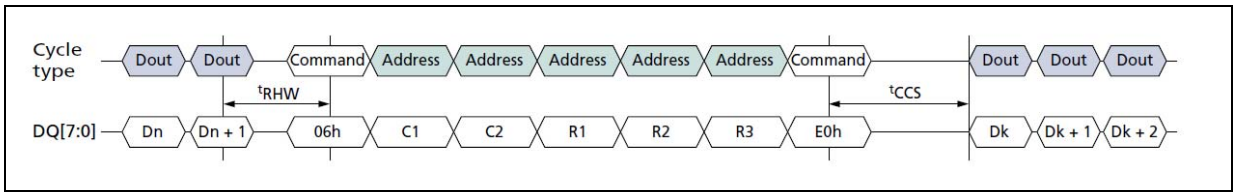
Following a multi-plane read page operation, the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select the cache register to be enabled for data output. After data output is complete on the selected plane, the command can be issued again to begin data output on another plane.

In devices with more than one die (LUN) per target, after all of the die (LUNs) on the target are ready (RDY = 1), the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used following an interleaved die (multi-LUN) read operation. Die (LUNs) that are not addressed are deselected to avoid bus contention.

In devices with more than one die (LUN) per target, during interleaved die (multi-LUN) operations where more than one or more die (LUNs) are busy (RDY = 1; ARDY = 0 or RDY = 0; ARDY = 0), the READ STATUS ENHANCED (78h) command must be issued to the die (LUN) to be selected prior to issuing the CHANGE READ COLUMN ENHANCED (06h-E0h). In this situation, using the CHANGE READ COLUMN ENHANCED (06h-E0h) command without the READ STATUS ENHANCED (78h) command will result in bus contention, as two or more die (LUNs) could output data.

If there is a need to update the column address without selecting a new cache register or LUN, the CHANGE READ COLUMN (05h-E0h) command can be used instead.

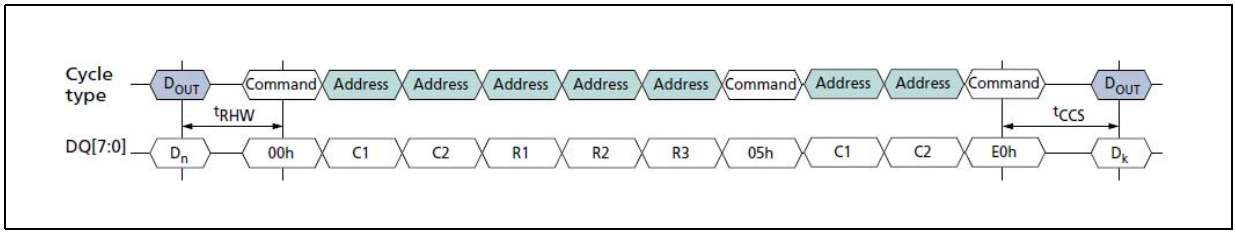
Figure 57. CHANGE READ COLUMN ENHANCED (06h-E0h) Operation



16.3 CHANGE READ COLUMN ENHANCED (00h-05h-E0h) Operation

This operation behaves the same as the CHANGE READ COLUMN ENHANCED (06h-E0h) command.

Figure 58. CHANGE READ COLUMN ENHANCED (00h-05h-E0h) Operation



16.4 CHANGE WRITE COLUMN (85h)

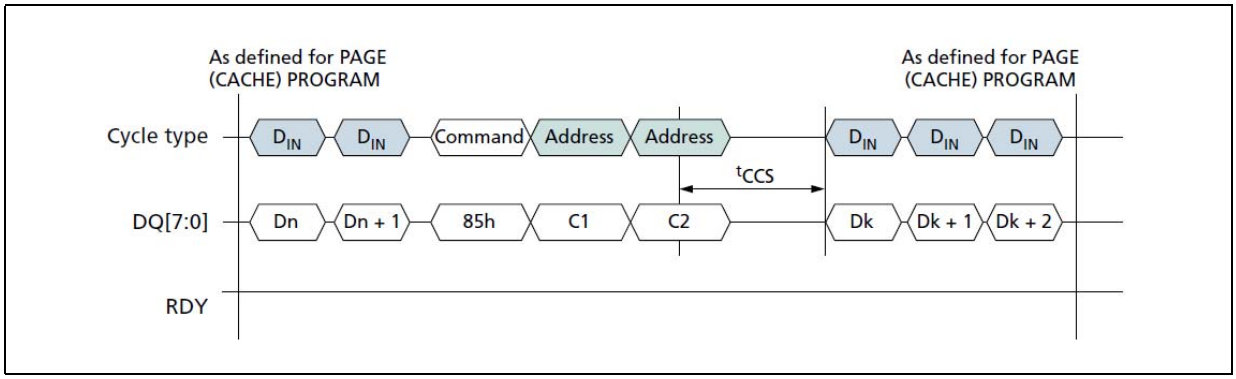
The CHANGE WRITE COLUMN (85h) command changes the column address of the selected cache register and enables data input on the last-selected die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache program operations (RDY = 1; ARDY = 0).

Writing 85h to the command register, followed by two column address cycles containing the column address, puts the selected die (LUN) into data input mode. After the second address cycle is issued, the host must wait at least tCCS before inputting data. The selected die (LUN) stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE WRITE COLUMN (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h).

In devices that have more than one die (LUN) per target, the CHANGE WRITE COLUMN (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

Figure 59. CHANGE WRITE COLUMN (85h) Operation



16.5 CHANGE ROW ADDRESS (85h)

The CHANGE ROW ADDRESS (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND Flash array. It also changes the column address of the selected cache register and enables data input on the specified die (LUN). This command is accepted by the selected die (LUN) when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected die (LUN) during cache programming operations (RDY = 1; ARDY = 0).

Write 85h to the command register. Then write two column address cycles and three row address cycles. This updates the page and block destination of the selected plane for the addressed LUN and puts the cache register into data input mode. After the fifth address cycle is issued the host must wait at least tCCS before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE ROW ADDRESS (85h) command is allowed after the required address cycles are specified, but prior to the final command cycle (10h, 11h, 15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h), PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE CACHE (80h-15h), COPYBACK PROGRAM (85h-10h), and COPYBACK PROGRAM MULTI-PLANE (85h-11h). When used with these commands, the LUN address and plane select bits are required to be identical to the LUN address and plane select bits originally specified.

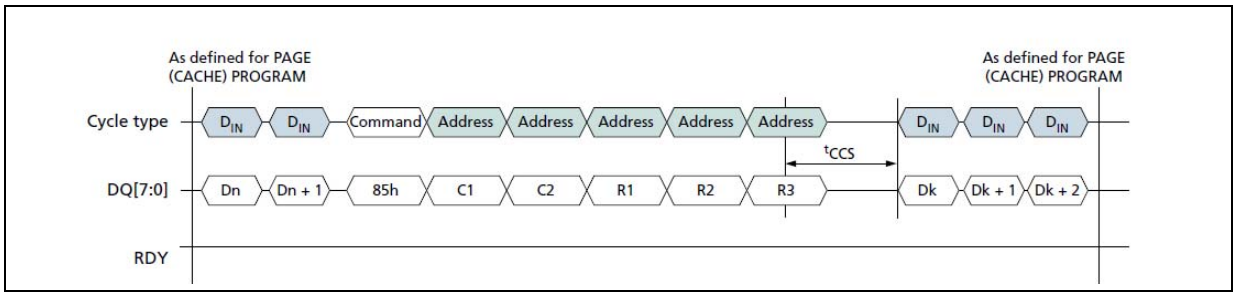
The CHANGE ROW ADDRESS (85h) command enables the host to modify the original page and block address for the data in the cache register to a new page and block address.

In devices that have more than one die (LUN) per target, the CHANGE ROW ADDRESS (85h) command can be used with other commands that support interleaved die (multi-LUN) operations.

The CHANGE ROW ADDRESS (85h) command can be used with the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) commands to read and modify cache register contents in small sections prior to programming cache register contents to the NAND Flash array. This capability can reduce the amount of buffer memory used in the host controller.

To modify the cache register contents in small sections, first issue a PAGE READ (00h-30h) or COPYBACK READ (00h-35h) operation. When data output is enabled, the host can output a portion of the cache register contents. To modify the cache register contents, issue the 85h command, the column and row addresses, and input the new data. The host can re-enable data output by issuing the 11h command, waiting tDBSY, and then issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command. It is possible toggle between data output and data input multiple times. After the final CHANGE ROW ADDRESS (85h) operation is complete, issue the 10h command to program the cache register to the NAND Flash array.

Figure 60. CHANGE ROW ADDRESS (85h) Operation



17.0 Read Operations

Read operations are used to copy data from the NAND Flash array of one or more of the planes to their respective cache registers and to enable data output from the cache registers to the host through the DQ bus.

17.1 Read Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND Flash array to its cache register and enables data output for that cache register.

During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h).

17.2 Read Cache Operations

To increase data throughput, the READ PAGE CACHE-series (31h, 00h-31h) commands can be used to output data from the cache register while concurrently copying a page from the NAND Flash array to the data register.

To begin a read page cache sequence, begin by reading a page from the NAND Flash array to its corresponding cache register using the READ PAGE (00h-30h) command. R/B# goes LOW during tR and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After tR (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h)—copies the next sequential page from the NAND Flash array to the data register
- READ PAGE CACHE RANDOM (00h-31h)—copies the page specified in this command from the NAND Flash array (any plane) to its corresponding data register

After the READ PAGE CACHE-series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for tRCBSY while the next page begins copying data from the array to the data register. After tRCBSY, R/B# goes HIGH and the die's (LUN's) status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache register becomes available and the page requested in the READ PAGE CACHE operation is transferred to the data register.

At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output by the die (LUN).

After outputting the desired number of bytes from the cache register, either an additional READ PAGE CACHE-series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for tRCBSY while the data register is copied into the cache register. After tRCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache register is available and that the die (LUN) is ready.

Data can then be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, tRCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), READ PAGE CACHE-series (31h, 00h-31h), CHANGE READ COLUMN (05h-E0h), and RESET (FFh, FCh).

17.3 Multi-Plane Read Operations

Multi-plane read page operations improve data throughput by copying data from more than one plane simultaneously to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the READ PAGE (00h-30h) command.

When the die (LUN) is ready, the CHANGE READ COLUMN ENHANCED (06h-E0h) command determines which plane outputs data. During data output, the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h) and CHANGE ROW ADDRESS (85h). See Section 21.0, “Multi-Plane Operations” on page 111 for details.

Multi-Plane Read Cache Operations

Multi-plane read cache operations can be used to output data from more than one cache register while concurrently copying one or more pages from the NAND Flash array to the data register. This is done by prepending READ PAGE MULTI-PLANE (00h-32h) commands in front of the PAGE READ CACHE RANDOM (00h-31h) command.

To begin a multi-plane read page cache sequence, begin by issuing a MULTI-PLANE READ PAGE operation using the READ PAGE MULTI-PLANE (00h-32h) and READ PAGE (00h-30h) commands. R/B# goes LOW during tR and the selected die (LUN) is busy (RDY = 0, ARDY = 0). After tR (R/B# is HIGH and RDY = 1, ARDY = 1), issue either of these commands:

- READ PAGE CACHE SEQUENTIAL (31h)—copies the next sequential page from the previously addressed planes from the NAND Flash array to the data registers.
- READ PAGE MULTI-PLANE (00h-32h) commands, if desired, followed by the READ PAGE CACHE RANDOM (00h-31h) command—copies the pages specified from the NAND Flash array to the corresponding data registers.

After the READ PAGE CACHE-series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for tRCBSY while the next pages begin copying data from the array to the data registers. After tRCBSY, R/B# goes HIGH and the LUN’s status register bits indicate the device is busy with a cache operation (RDY = 1, ARDY = 0). The cache registers become available and the pages requested in the READ PAGE CACHE operation are transferred to the data registers.

Issue the CHANGE READ COLUMN ENHANCED (06h-E0h) command to determine which cache register will output data. After data is output, the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used to output data from other cache registers. After a cache register has been selected, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output.

After outputting data from the cache registers, either an additional MULTI-PLANE READ CACHE-series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, and RDY = 0 and ARDY = 0 on the die (LUN) for tRCBSY while the data registers are copied into the cache registers. After ^{t}RCBSY, R/B# goes HIGH and RDY = 1 and ARDY = 1, indicating that the cache registers are available and that the die (LUN) is ready. Issue the CHANGE READ COLUMN ENHANCED (06h-E0h) command to determine which cache register will output data. After data is output, the CHANGE READ COLUMN ENHANCED (06h-E0h) command can be used to output data from other cache registers.

After a cache register has been selected, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the die (LUN) busy time, ^{t}RCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), multi-plane read cache-series (31h, 00h-32h, 00h-31h), CHANGE READ COLUMN (05h-E0h, 06h-E0h), and RESET (FFh, FCh).

See Section 21.0, “Multi-Plane Operations” on page 111 for additional multi-plane addressing requirements.

17.4 READ MODE (00h)

The READ MODE (00h) command disables status output and enables data output for the last-selected die (LUN) and cache register after a READ operation (00h-30h, 00h-35h) has been monitored with a status operation (70h, 78h). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 3Fh, 00h-31h) operations (RDY = 1 and ARDY = 0).

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to issuing the READ MODE (00h) command. This prevents bus contention.

17.5 READ PAGE (00h-30h)

The READ PAGE (00h–30h) command copies a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To read a page from the NAND Flash array, write the 00h command to the command register, the write five address cycles to the address registers, and conclude with the 30h command. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for ^{t}R as data is transferred.

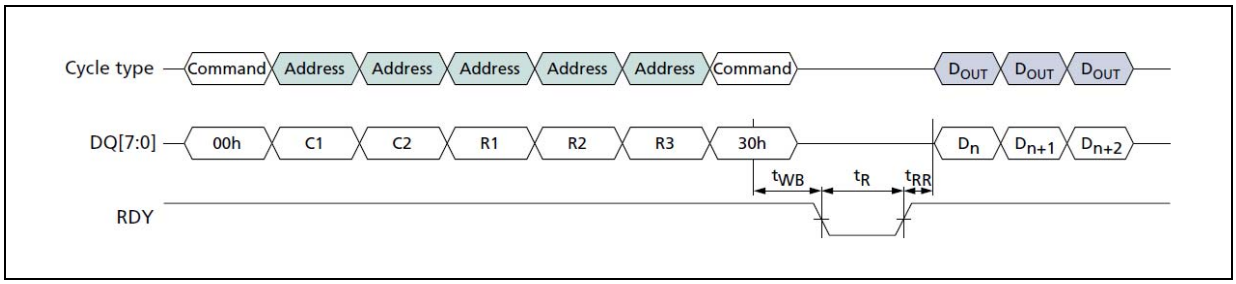
To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. If the status operations are used to monitor the LUN's status, when the die (LUN) is ready (RDY = 1, ARDY = 1), the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, output begins at the column address specified. During data output the CHANGE READ COLUMN (05h-E0h) command can be issued.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) prior to the issue of the READ MODE (00h) command. This prevents bus contention.

The READ PAGE (00h-30h) command is used as the final command of a multi-plane read operation. It is preceded by one or more READ PAGE MULTI-PLANE (00h-32h) commands. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the plane addressed in the READ PAGE (00h-30h) command. When the host requests data output, output begins at the column address last specified in the READ PAGE (00h-30h) command.

The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to enable data output in the other cache registers. See Multi-Plane Operations for additional multi-plane addressing requirements.

Figure 61. READ PAGE (00h-30h) Operation



17.6 READ PAGE CACHE SEQUENTIAL (31h)

The READ PAGE CACHE SEQUENTIAL (31h) command reads the next sequential page within a block into the data register while the previous page is output from the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

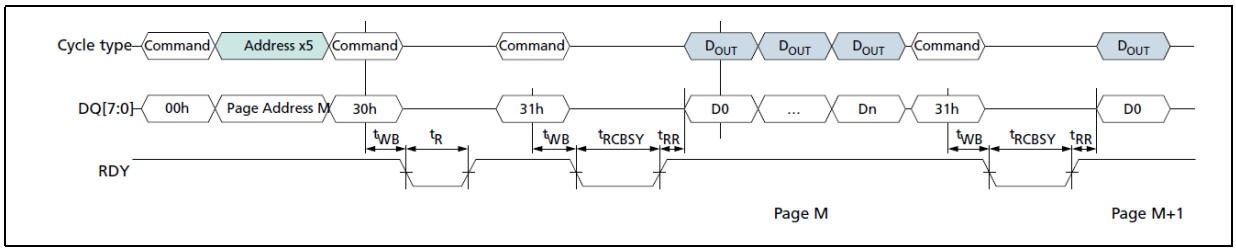
To issue this command, write 31h to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for tRCBSY. After tRCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register. At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

The READ PAGE CACHE SEQUENTIAL (31h) command can be used to cross block boundaries. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a block is read into the data register, the next page read will be the next logical block in the plane which the 31h command was issued. Do not issue the READ PAGE CACHE SEQUENTIAL (31h) to cross die (LUN) boundaries. Instead, issue the READ PAGE CACHE LAST (3Fh) command.

If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after a MULTIPLANE READ PAGE operation (00h-32h, 00h-30h), the next sequential pages are read into the data registers while the previous pages can be output from the cache registers.

After the die (LUN) is ready (RDY = 1, ARDY = 0), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

Figure 62. READ PAGE CACHE SEQUENTIAL (31h) Operation



17.7 READ PAGE CACHE RANDOM (00h-31h)

The READ PAGE CACHE RANDOM (00h-31h) command reads the specified block and page into the data register while the previous page is output from the cache register.

This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue this command, write 00h to the command register, then write five address cycles to the address register, and conclude by writing 31h to the command register. The column address in the address specified is ignored. The die (LUN) address must match the same die (LUN) address as the previous READ PAGE (00h-30h) command or, if applicable, the previous READ PAGE CACHE RANDOM (00h-31h) command. There is no restriction on the plane address.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY. After ^{t}RCBSY, R/B# goes HIGH and the die (LUN) is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register.

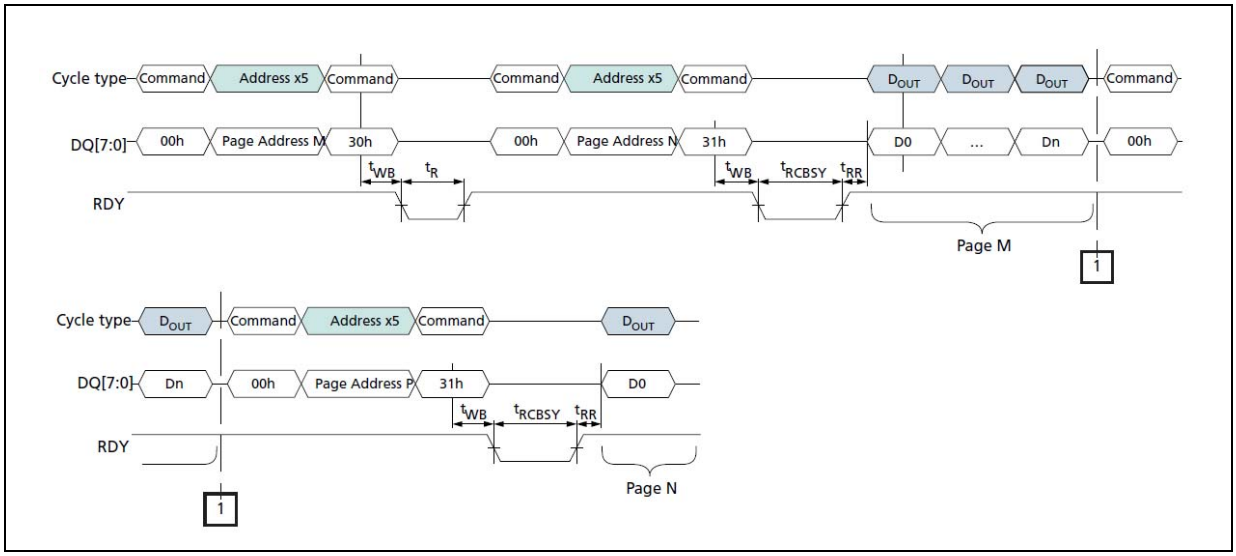
At this point, data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

If a MULTI-PLANE CACHE RANDOM (00h-32h, 00h-31h) command is issued after a MULTI-PLANE READ PAGE operation (00h-32h, 00h-30h), then the addressed pages are read into the data registers while the previous pages can be output from the cache registers.

After the die (LUN) is ready (RDY = 1, ARDY = 0), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

Figure 63. READ PAGE CACHE RANDOM (00h-31h) Operation



17.8 READ PAGE CACHE LAST (3Fh)

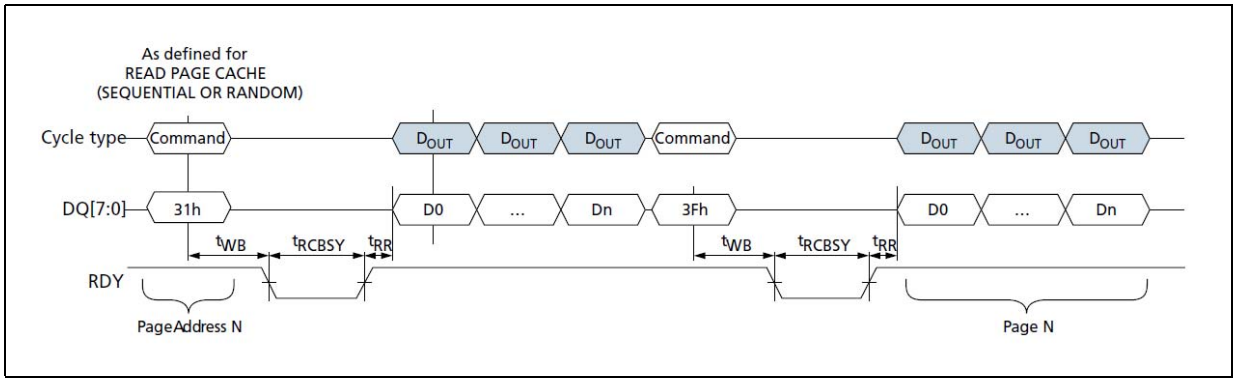
The READ PAGE CACHE LAST (3Fh) command ends the read page cache sequence and copies a page from the data register to the cache register. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

To issue the READ PAGE CACHE LAST (3Fh) command, write 3Fh to the command register. After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for tRCBSY. After tRCBSY, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one LUN per target, during and following interleaved die (multi-LUN) operations the READ STATUS ENHANCED (78h) command followed by the READ MODE (00h) command must be used to select only one die (LUN) and prevent bus contention.

If the READ PAGE CACHE LAST (3Fh) command is issued after a MULTI-PLANE READ PAGE CACHE operation (31h; 00h-32h, 00h-30h), the die (LUN) goes busy untIl the pages are copied from the data registers to the cache registers. After the die (LUN) is ready (RDY = 1, ARDY = 1), the CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to select which cache register outputs data.

Figure 64. READ PAGE CACHE LAST (3Fh) Operation



17.9 READ PAGE MULTI-PLANE (00h-32h)

The READ PAGE MULTI-PLANE (00h-32h) command queues a plane to transfer data from the NAND flash array to its cache register. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for data transfer. The READ PAGE (00h-30h) command is issued to select the final plane and to begin the read operation for all previously queued planes. All queued planes will transfer data from the NAND Flash array to their cache registers.

To issue the READ PAGE MULTI-PLANE (00h-32h) command, write 00h to the command register, then write five address cycles to the address register, and conclude by writing 32h to the command register. The column address in the address specified is ignored.

After this command is issued, R/B# goes LOW and the die (LUN) is busy (RDY = 0, ARDY = 0) for tDBSY. After ^{t}DBSY, R/B# goes HIGH and the die (LUN) is ready (RDY = 1, ARDY = 1). At this point, the die (LUN) and block are queued for data transfer from the array to the cache register for the addressed plane. During ^{t}DBSY, the only valid commands are status operations (70h, 78h) and reset commands (FFh, FCh). Following tDBSY, to continue the MULTI-PLANE READ operation, the only valid commands are status operations (70h, 78h), READ PAGE MULTI-PLANE (00h-32h), READ PAGE (00h-30h), and READ PAGE CACHE RANDOM (00h-31h).

Additional READ PAGE MULTI-PLANE (00h-32h) commands can be issued to queue additional planes for data transfer.

If the READ PAGE (00h-30h) command is used as the final command of a MULTIPLANE READ operation, data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the die (LUN) is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the last even plane addressed. When the host requests data output, it begins at the column address specified in the READ PAGE (00h-30h) command. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command.

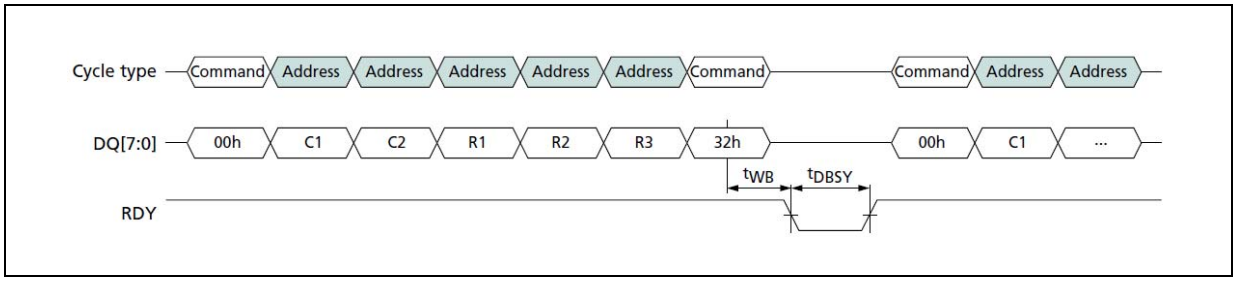
Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

If the READ PAGE CACHE SEQUENTIAL (31h) is used as the final command of a MULTI-PLANE READ CACHE operation, data is copied from the previously read operation from each plane to each cache register and then data is transferred from the NAND Flash array for all previously addressed planes to their respective data registers. When the die (LUN) is ready (RDY = 1, ARDY = 0), data output is enabled. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to determine which cache register outputs data first. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

If the READ PAGE CACHE RANDOM (00h-31h) command is used as the final command of a MULTI-PLANE READ CACHE operation, data is copied from the previously read operation from the data register to the cache register and then data is transferred from the NAND Flash array for all of the addressed planes to their respective data registers. When the die (LUN) is ready (RDY = 1, ARDY = 0), data output is enabled. The CHANGE READ COLUMN ENHANCED (06h-E0h) command is used to determine which cache register outputs data first. To enable data output in the other cache registers, use the CHANGE READ COLUMN ENHANCED (06h-E0h) command. Additionally, the CHANGE READ COLUMN (05h-E0h) command can be used to change the column address within the currently selected plane.

See Section 21.0, “Multi-Plane Operations” on page 111 for additional multi-plane addressing requirements.

Figure 65. READ PAGE MULTI-PLANE (00h-32h) Operation



18.0 Program Operations

Program operations are used to move data from the cache or data registers to the NAND array of one or more planes. During a program operation the contents of the cache and/or data registers are modified by the internal control logic.

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (i.e. 0, 1, 2, 3, …). Programming pages out of order within a block is prohibited.

Program Operations

The PROGRAM PAGE (80h-10h) command, when not preceded by the PROGRAM PAGE MULTI-PLANE (80h-11h) command, programs one page from the cache register to the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that the operation has completed successfully.

Program Cache Operations

The PROGRAM PAGE CACHE (80h-15h) command can be used to improve program operation system performance. When this command is issued, the die (LUN) goes busy (RDY = 0, ARDY = 0) while the cache register contents are copied to the data register, and the die (LUN) is busy with a program cache operation (RDY = 1, ARDY = 0. While the contents of the data register are moved to the NAND Flash array, the cache register is available for an additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) command.

For PROGRAM PAGE CACHE-series (80h-15h) operations, during the die (LUN) busy times, tCBSY and tLPROG, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and reset (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during PROGRAM PAGE CACHE-series (80h-15h) operations are status operations (70h, 78h), PROGRAM PAGE CACHE (80h-15h), PROGRAM PAGE (80h-10h), CHANGE WRITE COLUMN (85h), CHANGE ROW ADDRESS (85h), and reset (FFh, FCh).

Multi-Plane Program Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve program operation system performance by enabling multiple pages to be moved from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE (80h-10h) command. See Section 21.0, “Multi-Plane Operations” on page 111 for details.

Multi-Plane Program Cache Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve program cache operation system performance by enabling multiple pages to be moved from the cache registers to the data registers and, while the pages are being transferred from the data registers to different planes of the NAND Flash array, free the cache registers to receive data input from the host. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE CACHE (80h-15h) command. See Section 21.0, “Multi-Plane Operations” on page 111 for details.

18.1 PROGRAM PAGE (80h-10h)

The PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and moves the data from the cache register to the specified block and page address in the array of the selected die (LUN). This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1). It is also accepted by the die (LUN) when it is busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

To input a page to the cache register and move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified.

At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 10h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for tPROG as data is transferred.

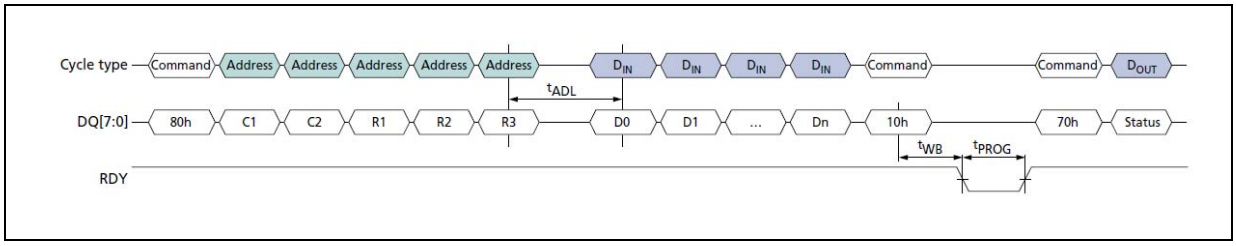
To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) may be used. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The PROGRAM PAGE (80h-10h) command is used as the final command of a multiplane program operation. It is preceded by one or more PROGRAM PAGE MULTIPLANE (80h-11h) commands. Data is transferred from the cache registers for all of the addressed planes to the NAND array. The host should check the status of the operation by using the status operations (70h, 78h). See Section 21.0, “Multi-Plane Operations” on page 111 for multi-plane addressing requirements.

At least 32 bytes of valid data and it’s associated ECC data must be programmed to a page for the data to be considered valid by the device.

Figure 66. PROGRAM PAGE (80h-10h) Operation



18.2 PROGRAM PAGE CACHE (80h-15h)

The PROGRAM PAGE CACHE (80h-15h) command enables the host to input data to a cache register; copies the data from the cache register to the data register; then moves the data register contents to the specified block and page address in the array of the selected die (LUN). After the data is copied to the data register, the cache register is available for additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) commands. The PROGRAM PAGE CACHE (80h-15h) command is accepted by the die (LUN) when it is ready (RDY =1, ARDY = 1). It is also accepted by the die (LUN) when busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

To input a page to the cache register to move it to the NAND array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target.

Then write five address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands may be issued. When data input is complete, write 15h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for tCBSY to allow the data register to become available from a previous program cache operation, to copy data from the cache register to the data register, and then to begin moving the data register contents to the specified page and block address.

To determine the progress of tCBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is busy with a PROGRAM CACHE operation (RDY = 1, ARDY = 0), the host should check the status of the FAILC bit to see if a previous cache operation was successful.

If, after ^{t}CBSY, the host wants to wait for the program cache operation to complete, without issuing the PROGRAM PAGE (80h-10h) command, the host should monitor ARDY until it is 1. The host should then check the status of the FAIL and FAILC bits.

In devices with more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a multi-plane program cache operation. It is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands. Data for all of the addressed planes is transferred from the cache registers to the corresponding data registers, then moved to the NAND Flash array. The host should check the status of the operation by using the status operations (70h, 78h). See Section 21.0, “Multi-Plane Operations” on page 111 for multi-plane addressing requirements.

At least 32 bytes of valid data and it's associated ECC data must be programmed to a page for the data to be considered valid by the device.

Figure 67. PROGRAM PAGE CACHE (80h–15h) Operation (Start)

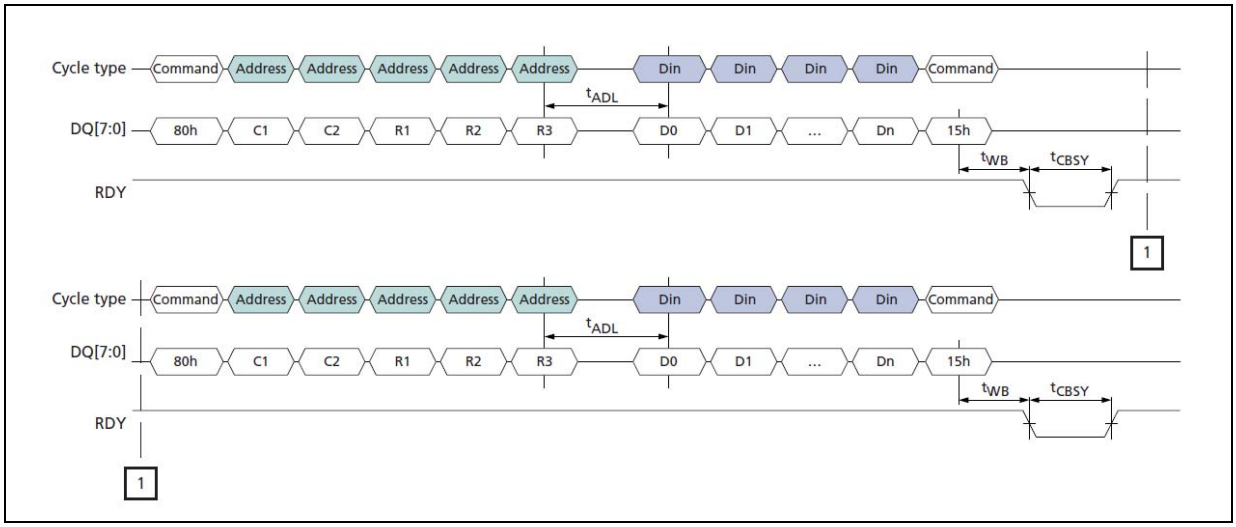
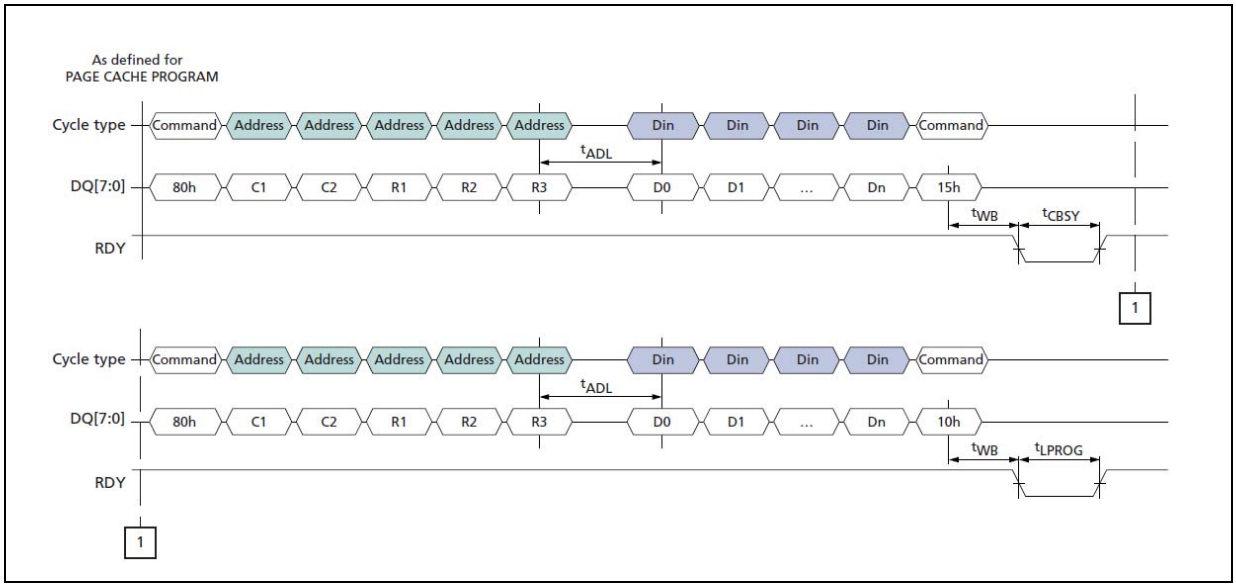


Figure 68. PROGRAM PAGE CACHE (80h–15h) Operation (End)



18.3 PROGRAM PAGE MULTI-PLANE (80h-11h)

The PROGRAM PAGE MULTI-PLANE (80h-11h) command enables the host to input data to the addressed plane's cache register and queue the cache register to ultimately be moved to the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the program operation for all previously queued planes, issue either the PROGRAM PAGE (80h-10h) command or the PROGRAM PAGE CACHE (80h-15h) command. All of the queued planes will move the data to the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1).

To input a page to the cache register and queue it to be moved to the NAND Flash array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by an 11h command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Write five address cycles containing the column address and row address; data input cycles follow.

Serial data is input beginning at the column address specified. At any time during the data input cycle, the CHANGE WRITE COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands can be issued. When data input is complete, write 11h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for tDBSY.

To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1), additional PROGRAM PAGE MULTI-PLANE (80h-11h) commands can be issued to queue additional planes for data transfer. Alternatively, the PROGRAM PAGE (80h-10h) or PROGRAM PAGE CACHE (80h-15h) commands can be issued.

When the PROGRAM PAGE (80h-10h) command is used as the final command of a multi-plane program operation, data is transferred from the cache registers to the NAND Flash array for all of the addressed planes during tPROG. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit for each of the planes to verify that programming completed successfully.

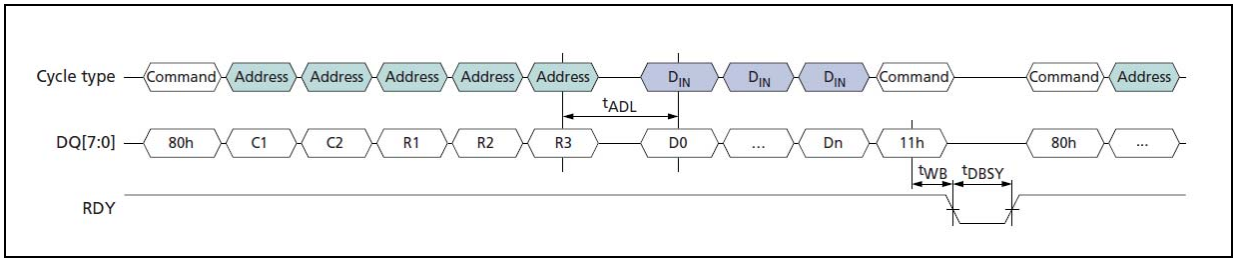
When the PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a MULTI-PLANE PROGRAM CACHE operation, data is transferred from the cache registers to the data registers after the previous array operations finish. The data is then moved from the data registers to the NAND Flash array for all of the addressed planes.

This occurs during tCBSY. After tCBSY, the host should check the status of the FAILC bit for each of the planes from the previous program cache operation, if any, to verify that programming completed successfully.

For the PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE (80h-10h), and PROGRAM PAGE CACHE (80h-15h) commands, see Section 21.0, “Multi-Plane Operations” on page 111 for multiplane addressing requirements.

At least 32 bytes of valid data and it’s associated ECC data must be programmed to a page for the data to be considered valid by the device.

Figure 69. PROGRAM PAGE MULTI-PLANE (80h–11h) Operation



For JEDEC compliance the PROGRAM PAGE MULTI-PLANE (81h-11h) command is also supported. This would also include the last command 81h-10h to conclude a PROGRAM PAGE MULTI-PLANE sequence and 81h-15h to conclude a PROGRAM PAGE CACHE MULTI-PLANE sequence.

19.0 Erase Operations

Erase operations are used to clear the contents of a block in the NAND Flash array to prepare its pages for program operations.

Erase Operations

The ERASE BLOCK (60h-D0h) command, when not preceded by the ERASE BLOCK MULTI-PLANE (60h-D1h) command, erases one block in the NAND Flash array. When the die (LUN) is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

MULTI-PLANE ERASE Operations

The ERASE BLOCK MULTI-PLANE (60h-D1h) command can be used to further system performance of erase operations by allowing more than one block to be erased in the NAND array. This is done by prepending one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands in front of the ERASE BLOCK (60h-D0h) command. See Section 21.0, “Multi-Plane Operations” on page 111 for details.

19.1 ERASE BLOCK (60h-D0h)

The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

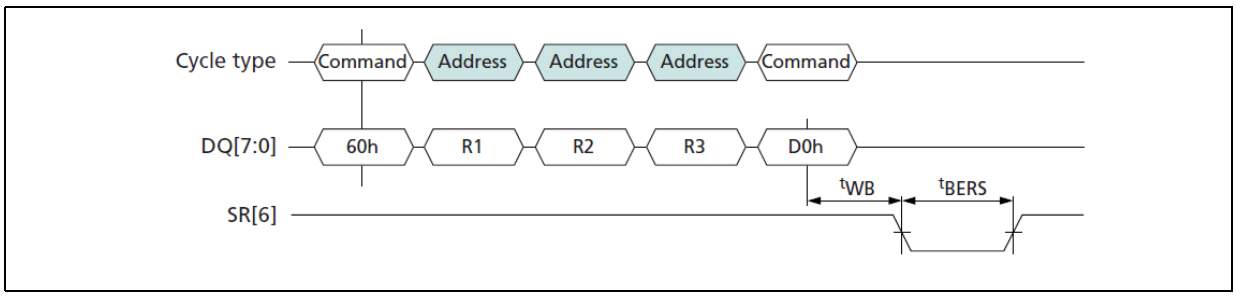
To erase a block, write 60h to the command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing D0h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for tBERS while the block is erased.

To determine the progress of an ERASE operation, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the die (LUN) is ready (RDY = 1, ARDY = 1) the host should check the status of the FAIL bit.

In devices that have more than one die (LUN) per target, during and following interleaved die (multi-LUN) operations, the READ STATUS ENHANCED (78h) command must be used to select only one die (LUN) for status output. Use of the READ STATUS (70h) command could cause more than one die (LUN) to respond, resulting in bus contention.

The ERASE BLOCK (60h-D0h) command is used as the final command of a MULTIPLANE ERASE operation. It is preceded by one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands. All of blocks in the addressed planes are erased. The host should check the status of the operation by using the status operations (70h, 78h). See Section 21.0, “Multi-Plane Operations” on page 111 for multi-plane addressing requirements.

Figure 70. ERASE BLOCK (60h-D0h) Operation



19.2 ERASE BLOCK MULTI-PLANE (60h-D1h)

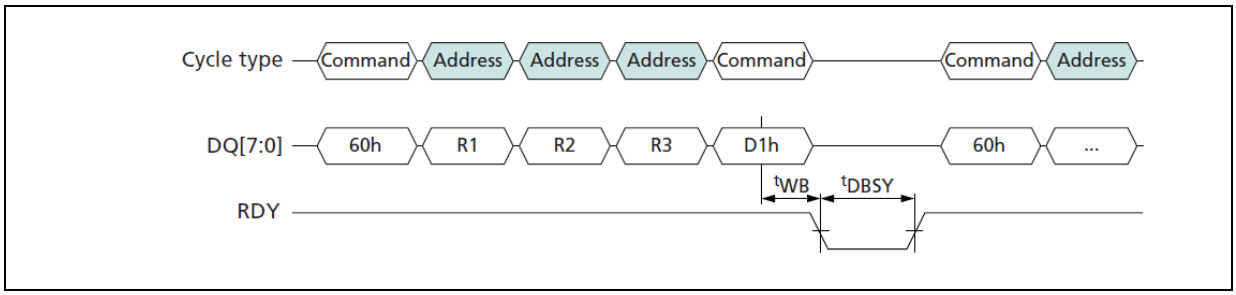
The ERASE BLOCK MULTI-PLANE (60h-D1h) command queues a block in the specified plane to be erased in the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for a block to be erased. To specify the final block to be erased and to begin the ERASE operation for all previously queued planes, issue the ERASE BLOCK (60h-D0h) command. This command is accepted by the die (LUN) when it is ready (RDY = 1, ARDY = 1).

To queue a block to be erased, write 60h to the command register, then write three address cycles containing the row address; the page address is ignored. Conclude by writing D1h to the command register. The selected die (LUN) will go busy (RDY = 0, ARDY = 0) for tDBSY.

To determine the progress of tDBSY, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1, ARDY = 1), additional ERASE BLOCK MULTI-PLANE (60h-D1h) commands can be issued to queue additional planes for erase. Alternatively, the ERASE BLOCK (60h-D0h) command can be issued to erase all of the queued blocks.

For multi-plane addressing requirements for the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Section 21.0, “Multi-Plane Operations” on page 111.

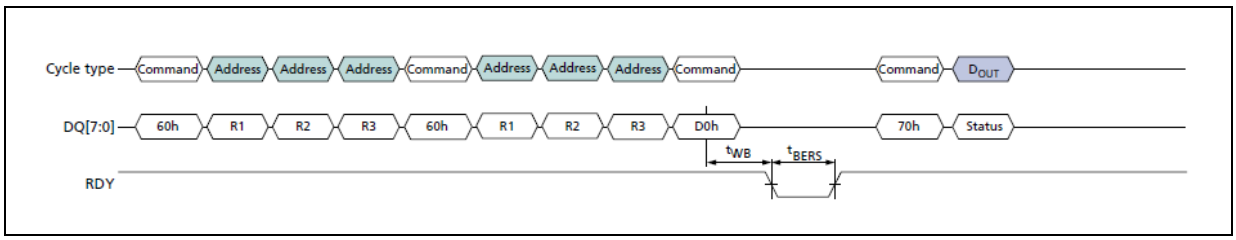
Figure 71. ERASE BLOCK MULTI-PLANE (60h–D1h) Operation



19.3 ERASE BLOCK MULTI-PLANE (60h-60h-D0h)

This operation behaves the same as the ERASE BLOCK MULTI-PLANE (60h-D1h) command followed by a ERASE BLOCK (60h-D0h) command.

Figure 72. ERASE BLOCK MULTI-PLANE (60h–60h-D0h) Operation



19.4 ERASE SUSPEND (61h)

The ERASE SUSPEND (61h) command is used to pause an erase in execution for the LUN specified (RDY =0, ARDY = 0). If ERASE SUSPEND (61h) is issued when ARDY = 1 or 0 and LUN is not performing an erase operation then the ERASE SUSPEND (61h) command should be ignored (i.e. tESPD = 0). If an interleaved erase is executing, the erase for all interleaved addresses is paused. The LUN shall make forward progress for the erase prior to suspending (e.g. complete an erase pulse). Since the erase is resumed from where it left off, an ERASE RESUME (D2h) on suspended block will count as one erase cycle.

FAIL (SR[0]) and SUSPEND (SR[2]) of the status register are valid for this command after RDY transitions from zero to one until the next transition of RDY to zero. SR[2] shall be set to one if an erase was suspended successfully, in this case SR[0] shall be cleared to zero. SR[2] shall be cleared to zero if the erase was completed, in this case SR[0] reflects whether the erase was successful.

To suspend a ongoing erase operation to a LUN, write 61h to the command register, then write three address cycles containing the row address; the page address is ignored.

The selected LUN status will be reflected in the status bits FAIL (SR[0]) and SUSPEND (SR[2]) in the status register after the status bit RDY (SR[6]) is set to one.

Table 25. ERASE SUSPEND (61h) Status Details

Description	SR[2]	SR[0]
ERASE completed with successful status	0	0
ERASE completed with fail status	0	1
ERASE suspended	1	0
Reserved	1	1

For multi-plane addressing requirements for the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see Section 21.0, “Multi-Plane Operations” on page 111.

To resume a suspended erase operation issue a D2h to the command register for the target which has had a erase operation suspended. The suspended erase operation will then resume and finish within tBERS.

While an erase is suspended, if the host issues a RESET (FFh), SYNCHRONOUS RESET (FCh), or RESET LUN (FAh) command for the affected LUN then the erase that was suspended is canceled and status is cleared. Commands accepted during suspended state include status (70h or 78h) commands, READ ID (90h), READ UNIQUE ID (EDh), GET FEATURES (EEh), and READ PARAMETER PAGE (ECh). and SET FEATURES (EFh). SET FEATURES (EFh) command is permitted, but not allowed for Feature Addresses that would change trims related to erase. MLBi commands are permitted, but not allowed for trims that would affect erase.

While an erase is suspended, if host issues a ERASE BLOCK (60h-D0h) command to the suspended block the suspended erase will be resumed (not restarted) and the erase that was suspended is canceled and status is cleared. If block erase is issued to different block address than suspended block then the erase is performed on the selected block and the erase that was suspended is canceled and status is cleared. If an erase is issued to a different LUN on the shared target then the erase is performed on the selected block and the erase that was suspended keeps it's suspend state.

Table 26. ERASE SUSPEND (61h) behavior for ERASE operations

Description	Command Issued	Next State
Block A erase operation suspended	ERASE BLOCK to Block A	Resume erase operation to Block A0
	ERASE BLOCK to Block B	Start normal erase to Block B and suspend to Block A is canceled
	ERASE BLOCK MULTI-PLANE to Block A and B	Start normal erase to Block A and B
ERASE BLOCK MULTI-PLANE to Block A and B suspended	ERASE BLOCK to Block A	Resume erase operation to Block A and B
	ERASE BLOCK to Block B	Resume erase operation to Block A and B
	ERASE BLOCK MULTI-PLANE to Block A and B	Resume erase operation to Block A and B
	ERASE BLOCK MULTI-PLANE to Block A and D	Start normal erase to block A and D. Suspend to Block B is canceled
	ERASE BLOCK MULTI-PLANE to Block C and B	Start normal erase to block C and B. Suspend to Block A is canceled.

While an erase is suspended, if host issues a program command to the suspended block or in the case of multi-plane program, if at least one of the blocks has a suspended erase, the program is aborted with short busy time (tESPDN) and the LOCK status (SR[7]) is set and the erase that was suspended keeps it's suspend state. If host issues a program command to block or LUN address other than the suspended block then the program is performed and the erase that was suspended keeps it's suspend state.

While an erase is suspended, if host issues a read command to the suspended block the read will be performed (undefined data read out) and the erase that was suspended keeps it's suspend state. If host issues read command to block or LUN address other than the suspended block then the read is performed and the erase that was suspended keeps it's suspend state.

If the host issues an ERASE SUSPEND (61h) or ERASE RESUME (D2h) while there is no erase operation ongoing or one that has been suspended respectively the NAND will respond with a tESPDN busy time.

Figure 73. ERASE SUSPEND (61h) Operation

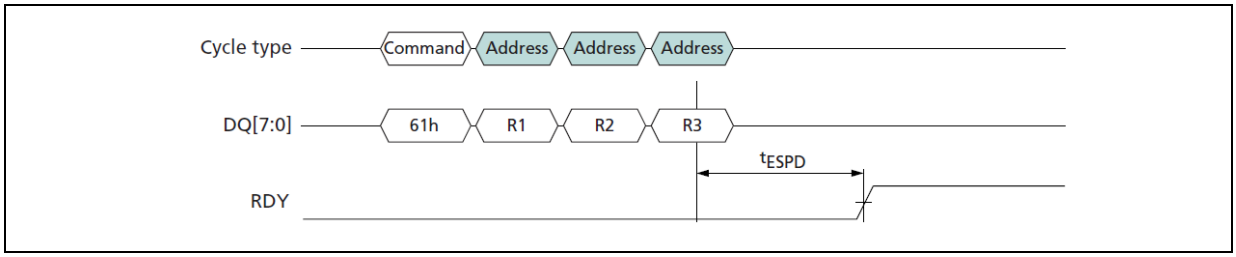
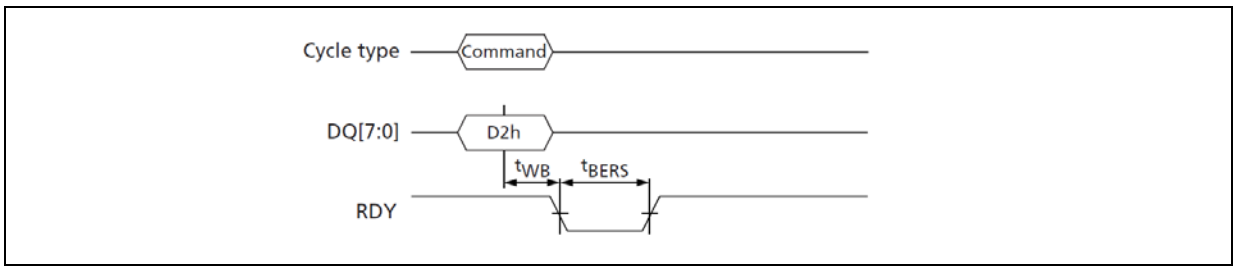


Figure 74. ERASE RESUME (D2h) Operation



20.0 Copyback Operations

COPYBACK operations make it possible to transfer data within a plane from one page to another using the cache register. This is particularly useful for block management and wear leveling.

The COPYBACK operation is a two-step process consisting of a COPYBACK READ (00h-35h) and a COPYBACK PROGRAM (85h-10h) command. To move data from one page to another on the same plane, first issue the COPYBACK READ (00h-35h) command.

When the die (LUN) is ready (RDY = 1, ARDY = 1), the host can transfer the data to a new page by issuing the COPYBACK PROGRAM (85h-10h) command. When the die (LUN) is again ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

To prevent bit errors from accumulating over multiple COPYBACK operations, it is recommended that the host read the data out of the cache register after the COPYBACK READ (00h-35h) completes prior to issuing the COPYBACK PROGRAM (85h-10h) command.

The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address. The host should check the data for ECC errors and correct them. When the COPYBACK PROGRAM (85h-10h) command is issued, any corrected data can be input. The CHANGE ROW ADDRESS (85h) command can be used to change the column address.

It is not possible to use the COPYBACK operation to move data from one plane to another or from one die (LUN) to another. Instead, use a READ PAGE (00h-30h) or COPYBACK READ (00h-35h) command to read the data out of the NAND, and then use a PROGRAM PAGE (80h-10h) command with data input to program the data to a new plane or die (LUN).

Between the COPYBACK READ (00h-35h) and COPYBACK PROGRAM (85h-10h) commands, the following commands are supported: status operations (70h, 78h), and column address operations (05h-E0h, 06h-E0h, 85h). Reset operations (FFh, FCh) can be issued after COPYBACK READ (00h-35h), but the contents of the cache registers on the target are not valid.

In devices which have more than one die (LUN) per target, once the COPYBACK READ (00h-35h) is issued, interleaved die (multi-LUN) operations are prohibited until after the COPYBACK PROGRAM (85h-10h) command is issued.

Multi-Plane Copyback Operations

Multi-plane copyback read operations improve read data throughput by copying data simultaneously from more than one plane to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the COPYBACK READ (00h-35h) command.

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command can be used to further system performance of COPYBACK PROGRAM operations by enabling movement of multiple pages from the cache registers to different planes of the NAND Flash array.

This is done by prepending one or more COPYBACK PROGRAM (85h-11h) commands in front of the COPYBACK PROGRAM (85h-10h) command. See Section 21.0, “Multi-Plane Operations” on page 111 for details.

20.1 COPYBACK READ (00h-35h)

The COPYBACK READ (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h. See "READ PAGE (00h-30h)" on page 91 for further details.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the COPYBACK PROGRAM (85h-10h) command to prevent the propagation of data errors.

Figure 75. COPYBACK READ (00h-35h) Operation

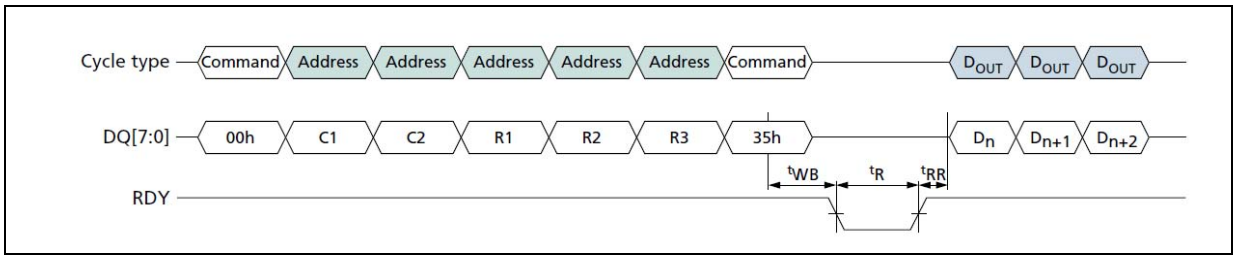
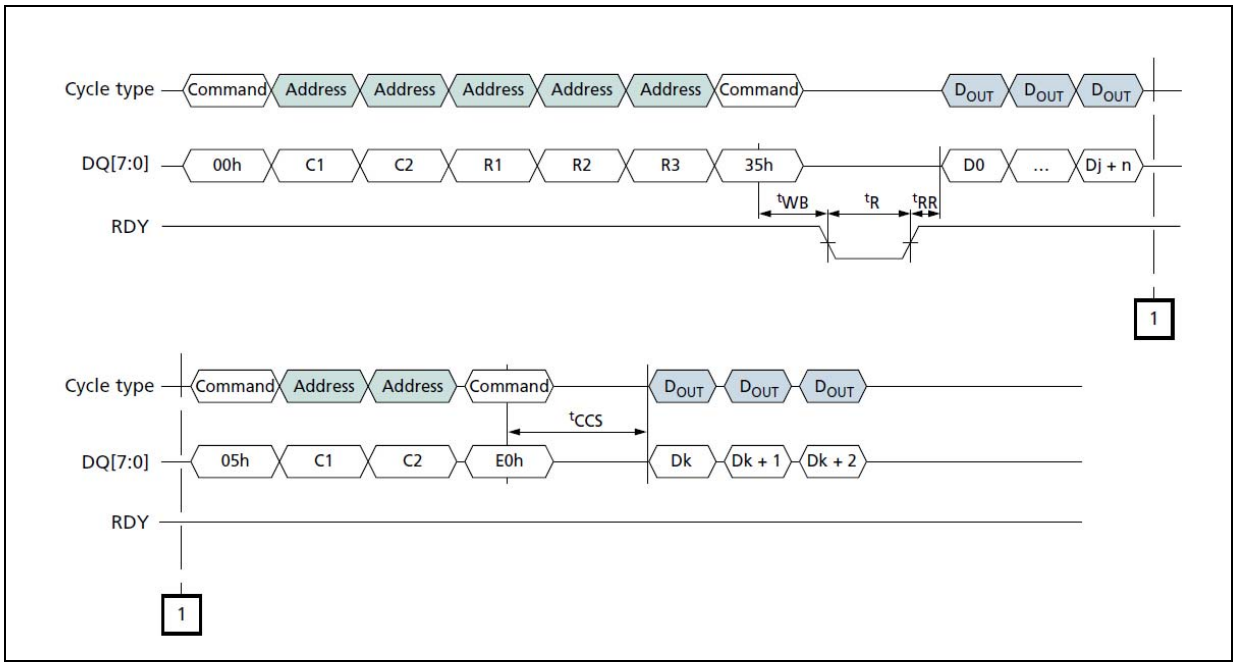


Figure 76. COPYBACK READ (00h–35h) with CHANGE READ COLUMN (05h–E0h) Operation



20.2 COPYBACK PROGRAM (85h–10h)

The COPYBACK PROGRAM (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, cache register contents are not cleared. See Section 18.1, “PROGRAM PAGE (80h-10h)” on page 98 for further details.

Figure 77. COPYBACK PROGRAM (85h–10h) Operation

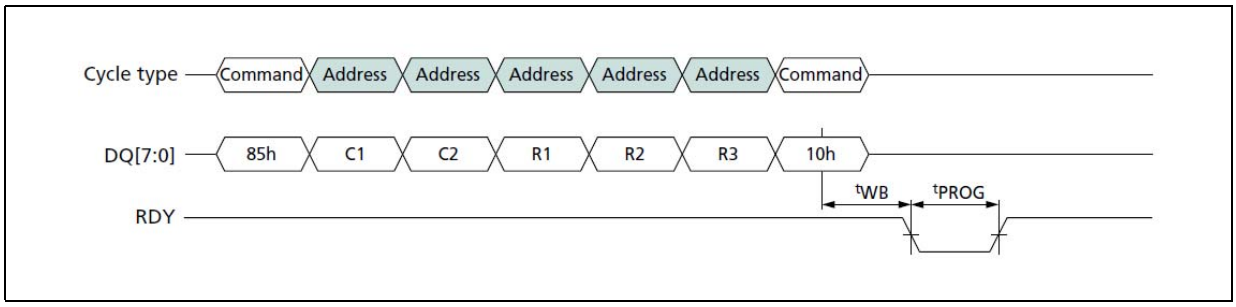
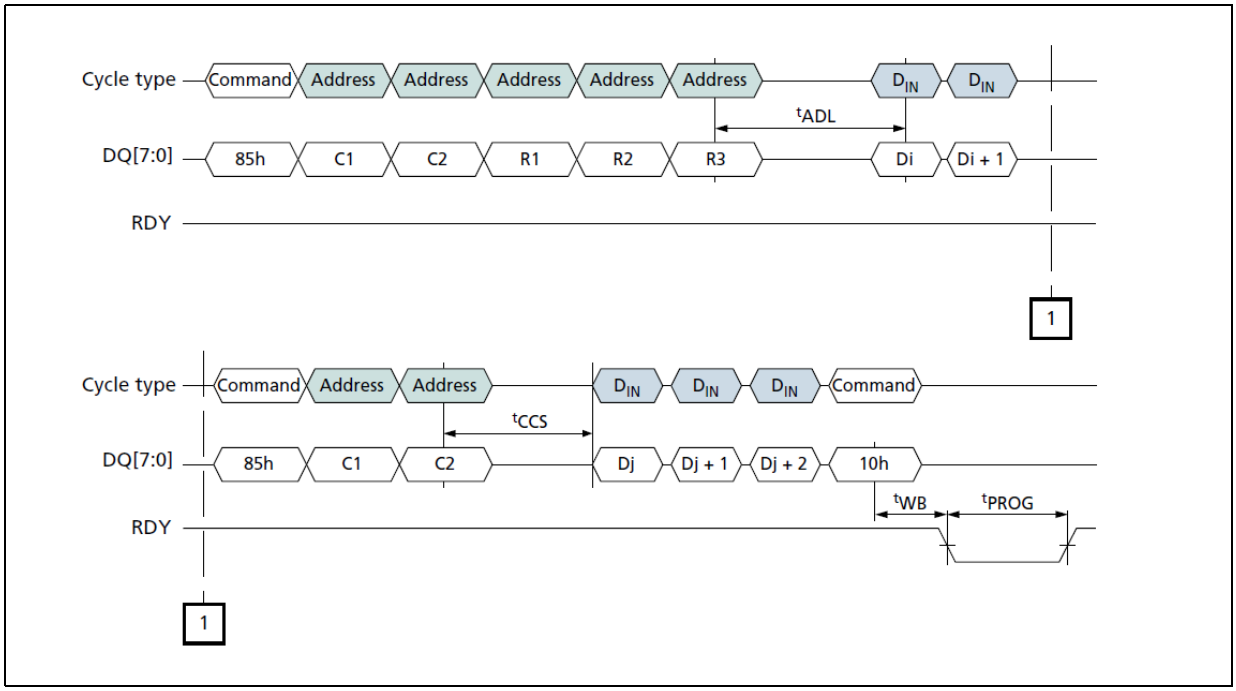


Figure 78. COPYBACK PROGRAM (85h-10h) with CHANGE WRITE COLUMN (85h) Operation



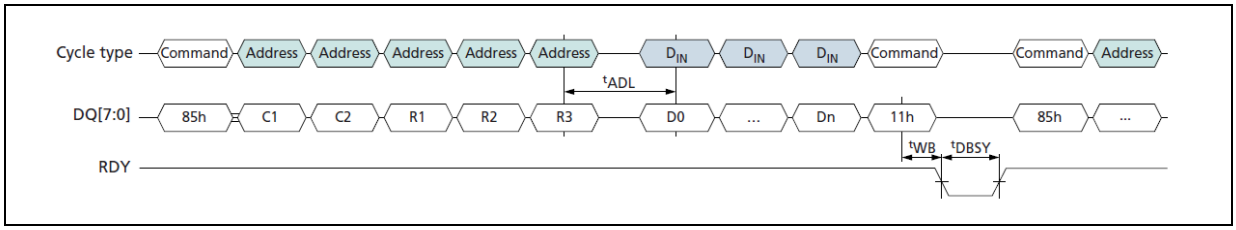
20.3 COPYBACK READ MULTI-PLANE (00h-32h)

The COPYBACK READ MULTI-PLANE (00h-32h) command is functionally identical to the READ PAGE MULTI-PLANE (00h-32h) command, except that the 35h command is written as the final command. The complete command sequence for the COPYBACK READ PAGE MULTI-PLANE is 00h-32h-00h-35h. See "READ PAGE MULTI-PLANE (00h-32h)" on page 95 for further details.

20.4 COPYBACK PROGRAM MULTI-PLANE (85h-11h)

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command is functionally identical to the PROGRAM PAGE MULTI-PLANE (80h-11h) command, except that when 85h is written to the command register, cache register contents are not cleared. See "PROGRAM PAGE MULTI-PLANE (80h-11h)" on page 101 for further details.

Figure 79. COPYBACK PROGRAM MULTI-PLANE (85h-11h) Operation



21.0 Multi-Plane Operations

Each NAND Flash logical unit (LUN) is divided into multiple physical planes. Each plane contains a cache register and a data register independent of the other planes. The planes are addressed via the low-order block address bits. Specific details are provided in Section 4.0, “Array Organization” on page 16.

Multi-plane operations make better use of the NAND Flash arrays on these physical planes by performing concurrent READ, PROGRAM, or ERASE operations on multiple planes, significantly improving system performance. Multi-plane operations must be of the same type across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

When issuing MULTI-PLANE PROGRAM or ERASE operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL = 1 and/or FAILC = 1), use the READ STATUS ENHANCED (78h) command—time for each plane—to determine which plane operation failed.

Multi-Plane Addressing

Multi-plane commands require an address per operational plane. For a given multiplane operation, these addresses are subject to the following requirements:

- The LUN address bit(s) must be identical for all of the issued addresses.
- The plane select bit, BA[9] for MLC and BA[8] for SLC, must be different for each issued address.
- The page address bits, PA[8:0] for MLC and PA[7:0] for SLC, must be identical for each issued address.

The READ STATUS (70h) command should be used following MULTI-PLANE PROGRAM PAGE and ERASE BLOCK operations on a single die (LUN).

Additional restrictions for 8KB page configurations

Additional addressing restrictions are required for devices configured as an 8KB page. Those additional addressing restrictions are:

- For COPYBACK and Multi-Plane operations the most significant block address bit, BA[20] for MLC and BA[19] for SLC, must be identical.

22.0 Interleaved Die (Multi-LUN) Operations

In devices that have more than one die (LUN) per target, it is possible to improve performance by interleaving operations between the die (LUNs). An interleaved die (multi-LUN) operation is one that individual die (LUNs) involved may be in any combination of busy or ready status during operations.

Interleaved die (multi-LUN) operations are prohibited following RESET (FFh, FCh), identification (90h, ECh, EDh), and configuration (EEh, EFh) operations until ARDY =1 for all of the die (LUNs) on the target.

During an interleaved die (multi-LUN) operation, there are two methods to determine operation completion. The R/B# signal indicates when all of the die (LUNs) have finished their operations. R/B# remains LOW while any die (LUN) is busy. When R/B# goes HIGH, all of the die (LUNs) are idle and the operations are complete. Alternatively, the READ STATUS ENHANCED (78h) command can report the status of each die (LUN) individually.

If a die (LUN) is performing a cache operation, like PROGRAM PAGE CACHE (80h-15h), then the die (LUN) is able to accept the data for another cache operation when status register bit 6 is 1. All operations, including cache operations, are complete on a die when status register bit 5 is 1.

Use the READ STATUS ENHANCED (78h) command to monitor status for the addressed die (LUN). When multi-plane commands are used with interleaved die (multi-LUN) operations, the multi-plane commands must also meet the requirements, see "Multi-Plane Operations" on page 111 for details. After the READ STATUS ENHANCED (78h) command has been issued, the READ STATUS (70h) command may be issued for the previously addressed die (LUN).

See Command Definitions for the list of commands that can be issued while other die (LUNs) are busy.

During an interleaved die (multi-LUN) operation that involves a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation and a READ operation, the PROGRAM-series operation must be issued before the READ-series operation. The data from the READ-series operation must be output to the host before the next PROGRAM-series operation is issued. This is because the 80h command clears the cache register contents of all cache registers on all planes.

When issuing combinations of commands to multiple die (LUNs) (e.g. Reads to one die (LUN) and Programs to another die (LUN)) or Reads to one die (LUN) and Reads to another die (LUN)), after the READ STATUS ENHANCED (78h) command is issued to the selected die (LUN) a CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command shall be issued prior to any data output from the selected die (LUN).

23.0 Error Management

Each NAND Flash die (LUN) is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the die (LUNs) could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC.

Additional blocks can develop with use. However, the total number of available blocks per die (LUN) will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error-correction algorithms. This type of software environment ensures data integrity. Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table for the first spare area location and the bad-block mark.

System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device.

A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. To ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation
- Under typical conditions, use the minimum required ECC (see Table 28)
- Use bad-block management and wear-leveling algorithms

The first block (physical block address 00h) for each CE# is guaranteed to be valid with ECC when shipped from the factory.

Table 28. Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	1996
Total available blocks per LUN	2048
First spare area location	16,384
Bad-block mark	00h
Minimum required ECC	40-bit ECC per 1097 bytes of data

24.0 Output Drive Impedance

Because NAND Flash is designed for use in systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. There are four supported settings for the output drivers: 18 ohms, 25 ohms, 35 ohms, and 50 ohms.

The nominal output drive strength setting is the power-on default value. The host can select a different drive strength setting using the SET FEATURES (EFh) command.

The output impedance range from minimum to maximum covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal line.

Table 29. Output Drive Strength Test Conditions (V_{CCQ} = 1.7-1.95V)

Range	Process	Voltage	Temperature
Maximum	Fast-Fast	1.95V	-25°C
Nominal	Typical-Typical	1.8V	+25°C
Minimum	Slow-Slow	1.7V	+85°C

Table 30. Output Drive Strength Impedance Values (V_{CCQ} = 1.7–1.95V)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
18 Ohms	Rpd	V_{CCQ} x 0.2	8.7	14	19.5	ohms
		V_{CCQ} x 0.5	11.7	18	24.3	ohms
		V_{CCQ} x 0.8	14	23	31.5	ohms
	Rpu	V_{CCQ} x 0.2	14	23	31.5	ohms
		V_{CCQ} x 0.5	11.7	18	24.3	ohms
		V_{CCQ} x 0.8	8.7	14	19.5	ohms
25 Ohms	Rpd	V_{CCQ} x 0.2	11	18	25	ohms
		V_{CCQ} x 0.5	16.3	25	33.7	ohms
		V_{CCQ} x 0.8	20	31	42	ohms
	Rpu	V_{CCQ} x 0.2	20	31	42	ohms
		V_{CCQ} x 0.5	16.3	25	33.7	ohms
		V_{CCQ} x 0.8	11	18	25	ohms
35 Ohms	Rpd	V_{CCQ} x 0.2	17	27.5	38	ohms
		V_{CCQ} x 0.5	22.7	35	17.3	ohms
		V_{CCQ} x 0.8	28	45	62	ohms
	Rpu	V_{CCQ} x 0.2	28	45	62	ohms
		V_{CCQ} x 0.5	22.7	35	47.3	ohms
		V_{CCQ} x 0.8	17	27.5	38	ohms
50 Ohms	Rpd	V_{CCQ} x 0.2	23	37.5	52	ohms
		V_{CCQ} x 0.5	32.5	50	67.5	ohms
		V_{CCQ} x 0.8	40	64	88	ohms
	Rpu	V_{CCQ} x 0.2	40	64	88	ohms
		V_{CCQ} x 0.5	32.5	50	67.5	ohms
		V_{CCQ} x 0.8	23	37.5	52	ohms

Table 31. Output Drive Strength Test Conditions (V_{CCQ} = 2.7-3.6V)

Range	Process	Voltage	Temperature
Maximum	Fast-Fast	3.6V	-40°C
Nominal	Typical-Typical	3.3V	+25°C
Minimum	Slow-Slow	2.7V	+85°C

Table 32. Output Drive Strength Impedance Values (V_{CCQ} = 2.7–3.6V)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
18 Ohms	Rpd	V_{CCQ} x 0.2	7.0	16.2	28.7	ohms
		V_{CCQ} x 0.5	9.0	18.0	36.0	ohms
		V_{CCQ} x 0.8	11.8	21.0	50.0	ohms
	Rpu	V_{CCQ} x 0.2	11.8	21.0	50.0	ohms
		V_{CCQ} x 0.5	9.0	18.0	36.0	ohms
		V_{CCQ} x 0.8	7.0	14.0	28.7	ohms
25 Ohms	Rpd	V_{CCQ} x 0.2	9.3	22.3	40.0	ohms
		V_{CCQ} x 0.5	12.6	25.0	50.0	ohms
		V_{CCQ} x 0.8	16.3	29.0	68.0	ohms
	Rpu	V_{CCQ} x 0.2	16.3	29.0	68.0	ohms
		V_{CCQ} x 0.5	12.6	25.0	68.0	ohms
		V_{CCQ} x 0.8	9.3	19.0	40.0	ohms
35 Ohms	Rpd	V_{CCQ} x 0.2	12.8	32.0	58.0	ohms
		V_{CCQ} x 0.5	18.0	35.0	70.0	ohms
		V_{CCQ} x 0.8	23.0	40.0	95.0	ohms
	Rpu	V_{CCQ} x 0.2	23.0	40.0	95.0	ohms
		V_{CCQ} x 0.5	18.0	35.0	70.0	ohms
		V_{CCQ} x 0.8	12.8	32.0	58.0	ohms
50 Ohms	Rpd	V_{CCQ} x 0.2	18.4	45.0	80.0	ohms
		V_{CCQ} x 0.5	25.0	50.0	100.0	ohms
		V_{CCQ} x 0.8	32.0	57.0	136.0	ohms
	Rpu	V_{CCQ} x 0.2	32.0	57.0	136.0	ohms
		V_{CCQ} x 0.5	25.0	50.0	100.0	ohms
		V_{CCQ} x 0.8	18.4	45.0	80.0	ohms

Table 33. Pull-Up and Pull-Down Output Impedance Mismatch for Asynchronous and Synchronous

Drive Strength	Minimum	Maximum	Unit	
18 Ohms	0	6.3	ohms	1,2
25 Ohms	0	8.8	ohms	1,2
35 Ohms	0	12.3	ohms	1,2
50 Ohms	0	17.5	ohms	1,2

Notes:
1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2. Test conditions: $V_{CCQ} = V_{CCQ}$ (MIN), $V_{OUT} = V_{CCQ} \times 0.5$, $T_A = T_{OPER}$.

Table 34. Pull-Up and Pull-Down Output Impedance Mismatch for Synchronous

Drive Strength	Minimum	Maximum	Unit	
18 Ohms	0	3.2	ohms	1,2
25 Ohms	0	4.4	ohms	1,2
35 Ohms	0	6.2	ohms	1,2
50 Ohms	0	8.8	ohms	1,2

Notes:
1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2. Test conditions: $V_{CCQ} = V_{CCQ}$ (MIN), $V_{OUT} = V_{CCQ} \times 0.5$, $T_A = T_{OPER}$.

25.0 AC Overshoot/Undershoot Specifications

The supported AC overshoot and undershoot area depends on the timing mode selected by the host.

Table 35. Asynchronous Overshoot/Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V
Maximum overshoot area above V_{CCQ}	3	3	3	3	3	3	V-ns
Maximum undershoot area above V_{CCQ}	3	3	3	3	3	3	V-ns

Table 36. Onfi 2.3 Overshoot/Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V
Maximum overshoot area above V_{CCQ}	3	3	3	2.25	1.8	1.5	V-ns
Maximum undershoot area below V_{CCQ}	3	3	3	2.25	1.8	1.5	V-ns

Table 37. Onfi 3.0 Overshoot/Undershoot Parameters

Parameter	Signals	Timing Mode								Unit
		0	1	2	3	4	5			
Maximum peak amplitude provided for overshoot area	-	1	1	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	-	1	1	1	1	1	1	1	1	V
Maximum overshoot area above V_{CCQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	
Maximum undershoot area below V_{CCQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	

Figure 80. Overshoot

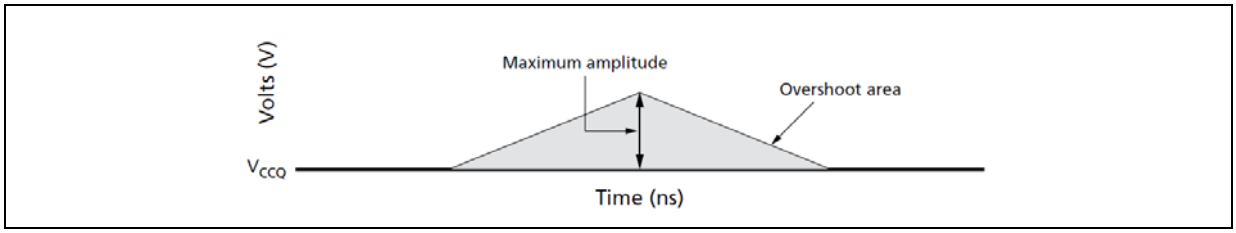
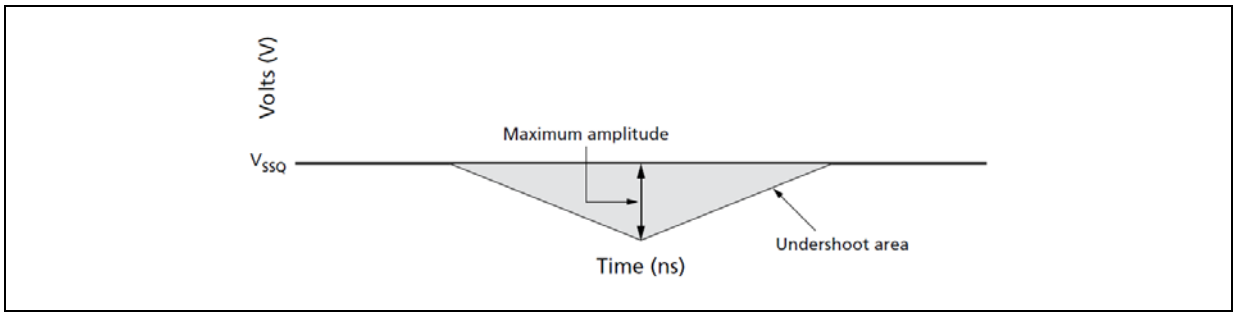


Figure 81. Undershoot



26.0 Input Slew Rate

Though all AC timing parameters are tested with a nominal input slew rate of 1 V/ns, it is possible to run the device at a slower slew rate. The input slew rates shown below are sampled, and not 100% tested. When using slew rates slower than the minimum values, timing must be derated by the host.

Table 38. Test Conditions for Input Slew Rate

Parameter	Value
Rising edge	$V_{IL(DC)}$ To $V_{IH(AC)}$ for Onfi 2.3 and $V_{IL(AC)}$ to $V_{IH(AC)}$ for Onfi 3.0
Falling edge	$V_{IL(DC)}$ To $V_{IH(AC)}$ for Onfi 2.3 and $V_{IL(AC)}$ to $V_{IH(AC)}$ for Onfi 3.0
Temperature Range	T_A

The minimum and maximum input slew rate requirements that the device shall comply with below for synchronous operations. If the input slew rate falls below the minimum value, then derating shall be applied.

Table 39. Synchronous Maximum and Minimum Input Slew Rate

Description	Timing Modes 0-5	Unit
Input slew rate (min)	0.5	V/ns
Input slew rate (max)	4.5	V/ns

The minimum and maximum input slew rate requirements that the device shall comply with below for onfi 3.0 operations.

Table 42. Onfi 3.0 Maximum and Minimum Input Slew Rate

Description	Single Ended	Differential	Unit
	Timing Modes 0-7	Timing Modes 0-7	
Input slew rate (min)	1.0	2.0	V/ns
Input slew rate (max)	4.5	9.0	V/ns

Δ

27.0 Output Slew Rate

The output slew rate is tested using the following setup with only one die per DQ channel.

Table 45. Test Conditions for Output Slew Rate

Parameter	Asynchronous / Synchronous 2.0 Interface	Onfi 3.0 single- ended[1]	Onfi 3.0 differential[1]
$V_{OL(DC)}$	0.3 x V_{CCQ}	-	
$V_{OH(DC)}$	0.7 x V_{CCQ}	-	
$V_{OL(AC)}$[2]	0.2 x V_{CCQ}	V_{TT} - (V_{CCQ} * 0.15)	
$V_{OH(AC)}$[2]	0.8 x V_{CCQ}	V_{TT} - (V_{CCQ} * 0.15)	-
$V_{OLdiff(AC)}$	-	-	-0.3 * V_{CCQ}
$V_{OHdiff(AC)}$	-	-	0.3 * V_{CCQ}
Rising edge (^{t}RISE)	$V_{OL(DC)}$ to $V_{OH(AC)}$	$V_{OL(DC)}$ to $V_{OH(AC)}$	-
Falling edge (^{t}FALL)	$V_{OH(DC)}$ to $V_{OL(AC)}$	$V_{OH(AC)}$ to $V_{OL(AC)}$	-
Differential rising edge (^{t}RISEdiff)	-	-	$V_{OLdiff(AC)}$ to $V_{OHdiff(AC)}$
Differential falling edge (^{t}FALLdiff)	-	-	$V_{OHdiff(AC)}$ to $V_{OLdiff(AC)}$
Output slew rate rising edge	[$V_{OH(AC)}$ - $V_{OL(DC)}$] / ^{t}RISE	[$V_{OH(AC)}$ - $V_{OL(AC)}$] / ^{t}RISE	[$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$] / ^{t}RISEdiff
Output reference load[2]	50 Ohm to V_{TT}	50 Ohm to V_{TT}	50 Ohm to V_{TT}
Temperature range	T_A	T_A	T_A

Notes:
1. 1.8V V_{CCQ} is required for Onfi 3.0 operations.
2. V_{TT} is 0.5 x V_{CCQ}.

28.0 Power Cycle Requirements

Upon power-down the NAND device requires a maximum voltage and minimum time that the host must hold V_{CC} and V_{CCQ} below the voltage prior to power-on.

Table 49. Power Cycle Requirements

Parameter	Value	Unit
Maximum V_{CC}/V_{CCQ}	100	mV
Minimum time below Maximum Voltage	100	ns

29.0 Electrical Specifications

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed.

Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 50. Absolute Maximum Ratings by Device

Parameter	Symbol	Min	Max	Unit
Voltage input	V_{IN}	–0.6	4.6	V
V_{CC} supply voltage	V_{CC}	–0.6	4.6	V
V_{CCQ} supply voltage	V_{CCQ}	-0.6	4.6	V
V_{PP} supply voltage	V_{PP}	TBD	TBD	V
V_{REFQ} supply voltage	V_{REFQ}	-0.6	4.6	V
Storage temperature	T_{STG}	-65	150	°C

Table 51. Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	70	°C
V_{CC} supply voltage		V_{CC}	2.7	3.3	3.6	V
V_{CCQ} supply voltage (1.8V)		V_{CCQ}	1.7	1.8	1.95	V
V_{CCQ} supply voltage (3.3V)			2.7	3.3	3.6	V
V_{PP} supply voltage (12V)		V_{PP}	11.5	12.0	12.5	V
V_{REFQ} supply voltage (1.8V)		V_{REFQ}	0.49 x V_{CCQ}	1.8	0.51 x V_{CCQ}	V
Vss ground voltage		Vss	0	0	0	V

Table 52. Valid Blocks per LUN

Parameter	Symbol	Min	Typ	Max	Unit
Valid block number	NVB	1998	2048	Blocks	1

Note: 1. Invalid blocks are blocks that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid from the factory.

Table 54. Test Conditions

Parameter	Asynchronous and Onfi 2.3	Onfi 3.0 single-ended	Onfi 3.0 differential	Notes
Rising input transition	$V_{IL(DC)}$ to $V_{IH(AC)}$	$V_{IL(DC)}$ to $V_{IH(AC)}$	$V_{ILdiff(DC)}$ max to $V_{IHdiff(AC)}$ min	1

Table 54. Test Conditions

Parameter	Asynchronous and Onfi 2.3	Onfi 3.0 single-ended	Onfi 3.0 differential	Notes
Falling input transition	$V_{IH(DC)}$ to $V_{IL(AC)}$	$V_{IH(DC)}$ to $V_{IHLAC)}$	$V_{IHdiff(DC)}$ max to $V_{ILdiff(AC)}$	1
Input rise and fall slew rates	1 V/ns	1 V/ns	2 V/ns	-
Input timing levels	$V_{CCQ}/2$	V_{REQ}	cross-point	1
Output timing levels	$V_{CCQ}/2$	V_{TT}	cross-point	
Output load: Nominal output drive strength	50 Ohm to V_{TT}	50 Ohm to V_{TT}	50 Ohm to V_{TT}	2,3,4

Notes:
1. The receiver will effectively switch as a result of the signal crossing the AC input level; it will remain in that status as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
2. Transmission line delay is assumed to be very small.
3. This test setup applies to all package configurations.
4. V_{TT} is 0.5 x V_{CCQ}.

30.0 Electrical Specifications — DC Characteristics and Operating Conditions (Asynchronous)

Table 55. DC Characteristics and Operating Characteristics (Asynchronous Interface)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Array read current (active)	-	I_{CC1_A}	–	25	50	mA
Array program current (active)	-	I_{CC1_A}	–	25	50	mA
Erase current (active)	–	I_{CC3_A}	–	25	50	mA
I/O burst read current	$^{t}RC = {}^{t}RC$ (MIN); I_{OUT} = 0mA	I_{CC4R_A}	–	5	10	mA
I/O burst write current	$^{t}WC = {}^{t}WC$ (MIN)	I_{CC4W_A}	–	3	5	mA
Bus idle current	–	I_{CC5_a}	–	3	5	mA
Current during first RESET command power-up	-	I_{CC6}	–	-	1-	µA
V_{PP} current (active)	During I_{CC1_A} or I_{CC2_A}	I_{PP}	–		5	mA
Standby current - V_{CC}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SB}		30	75	uA
Standby current - V_{CCQ}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SBQ}		3	10	uA
Staggered power-up current	$^{t}RISE$ = 1ms; C_{LINE} = 0.1uF	I_{ST}		-	10	uA

Note: 1. All values are per die (LUN) unless otherwise specified.

Table 56. DC Characteristics and Operating Characteristics (Onfi 2.3 and Onfi 3.0 Interfaces)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Array read current (active)	CE# = V_{IL} ; $^{t}CK = {}^{t}CK$ (MIN) Onfi 2.3	I_{CC1_S}	–	25	50	mA
Array program current (active)	$^{t}CK = {}^{t}CK$ (MIN) Onfi 2.3	I_{CC2_S}	–	25	50	mA
Erase current (active)	$^{t}CK = {}^{t}CK$ (MIN) Onfi 2.3	I_{CC3_S}	–	25	50	mA
I/O burst read current	$^{t}CK = {}^{t}CK$ (MIN) Onfi 2.3 $^{t}RC = {}^{t}RC$ (MIN) Onfi 3.0 I_{OUT} = 0mA	I_{CC4R_S}	–	10^{2} TBD[3]	20^{2} TBD[3]	mA
I/O burst write current	$^{t}CK = {}^{t}CK$ (MIN) Onfi 2.3; $^{t}CK = {}^{t}CK$ (MIN) Onfi 3.0	I_{CC4W_S}	–	10^{2} TBD[3]	20^{2} TBD[3]	mA
Bus idle current	CK = ^{t}CK (MIN) Onfi 2.3	I_{CC5_S}	–	5	10	mA
V_{PP} current (active)	During I_{CC1_A} or I_{CC2_A}	I_{PP}	–		5	mA
Standby current - V_{CC}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SB}		30	75	uA
Standby current - V_{CCQ}	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CCQ}	I_{SBQ}		3	10	uA

Notes:
1. All values are per die (LUN) unless otherwise specified.
2. For speeds up to 200MT/s.
3. For speeds greater than 200MT/s.

31.0 Electrical Specifications — DC Characteristics and Operating Conditions (V_{CCQ})

Table 57. Asynchronous/Onfi 2.3 DC Characteristics and Operating Conditions (1.8V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	CE#, DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#), WP#	$V_{IH(AC)}$	0.8 x V_{CCQ}	-	V_{CCQ} +0.3	V	
AC input low voltage		$V_{IL(AC)}$	-0.3	-	0.2 x V_{CCQ}	V	
DC input high voltage	DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (RE#)	$V_{IH(DC)}$	0.7 x V_{CCQ}	-	V_{CCQ} +0.3	mA	
DC input low voltage		$V_{IL(DC)}$	-0.3	-	0.3 x V_{CCQ}	V	
Input leakage current	Any input VIN = 0V to V_{CCQ} (all other pins under test = 0V)	I_L	–	-	±10	µA	1
I/O burst write current	^tCK = ^tCK (MIN) Onfi 2.3; ^tCK = ^tCK (MIN) Onfi 3.0	I_{CC4W_S}	–	10[2]	20[2]	mA	
				TBD[3]	TBD[3]		
Output leakage current	DQ are disabled; Vout = 0V to VCCQ	I_{LO}	-	-	±10	µA	1
Output low current	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	-	mA	2

Notes:
1. All leakage currents are per die (LUN). Two die (LUNs) have a maximum leakage current of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA.
2. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength.

Table 58. Onfi 3.0 DC Characteristics and Operating Conditions for Single-Ended Signals (1.8V V_{CCQ})

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	$V_{IH(AC)}$	V_{REFQ} + 0.250	-	-	V	
AC input low voltage		$V_{IL(AC)}$	-	-	V_{REFQ} + 0.250	V	
DC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	$V_{IH(DC)}$	V_{REFQ} + 0.125	-	V_{CCQ} + 0.3	V	2
DC input low voltage		$V_{IL(DC)}$	-0.3	-	V_{REFQ} + 0.125	V	2
Input leakage current	Any input V_{IN} = 0V to V_{CCQ} (all other pins under test = 0V)	I_L	–	-	±10	µA	1
Output leakage current	DQ are disabled; Vout = 0V to V_{CCQ}	I_{LO}	-	-	±10	µA	1
Output low current (R/B#)	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	-	mA	2

Notes:
1. All leakage currents are per die (LUN). Two die (LUNs) have a maximum leakage current of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA.
2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.
3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See (page 0) for additional details.

Table 59. Onfi 3.0 DC Characteristics and Operating Conditions for Differential Signals (1.8V V_{CCQ})

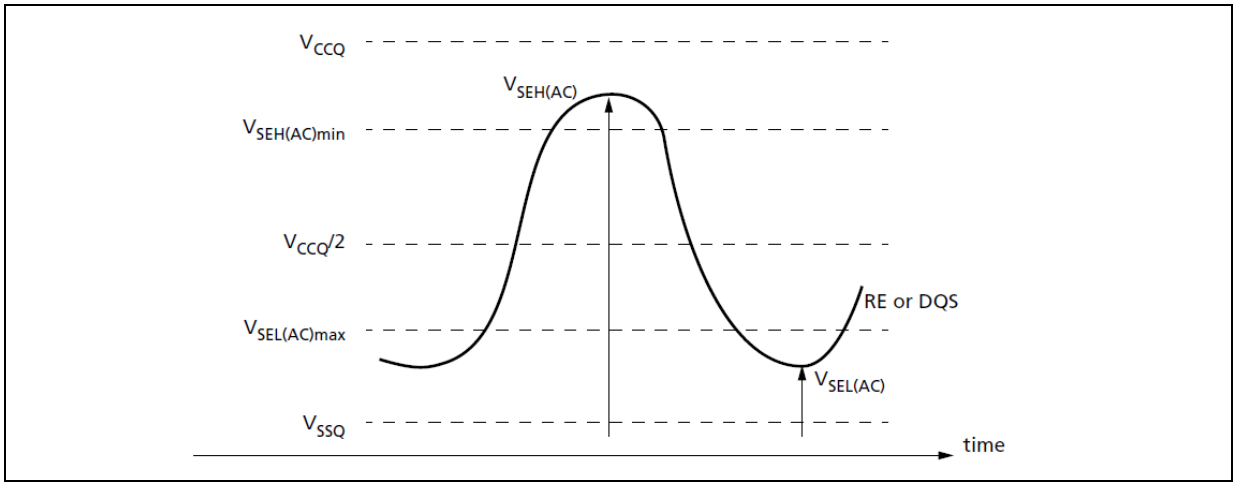
Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
Differential AC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	$V_{IHdiff\ (AC)}$	2 x [$V_{IH(DC)}$ - V_{REF}]	-	see note	V	2
Differential AC input low voltage		$V_{ILdiff\ (AC)}$	see note	-	2 x [V_{REF} - $V_{IL(AC)}$]	V	2
Differential DC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	$V_{IHdiff(DC)}$	2 x [$V_{IH(DC)}$ - V_{REF}]	-	see note	V	2
Differential DC input low voltage		$V_{ILdiff(DC)}$	see note	-	2 x [V_{REF} - $V_{IL(DC)}$]	V	2
Input leakage current	Any input V_{IN} = 0V to V_{CCQ} (all other pins under test = 0V)	I_L	–	-	±10	µA	1
Output leakage current	DQ are disabled; Vout = 0V to V_{CCQ}	I_{LO}	-	-	±10	µA	1
Output low current (R/B#)	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	-	mA	2

Notes:
1. All leakage currents are per die (LUN). Two die (LUNs) have a maximum leakage current of ±20µA and four die (LUNs) have a maximum leakage current of ±40µA.
2. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.
3. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength.

31.1 Single-Ended Requirements for Differential signals

Each individual component of a differential signal (RE_t, RE_c, DQS_t, or DQS_c) shall comply with requirements for single-ended signals. RE_t and RE_c shall meet $V_{SEH(AC)}$ Min / $V_{SEL(AC)}$ Max in every half-cycle. DQS_t and DQS_c shall meet $V_{SEH(AC)}$ Min / $V_{SEL(AC)}$ Max in every half-cycle preceeding and following a valid transition.

Figure 82. Single-Ended requirements for Differential Signals



While control (for example, ALE, CLE) and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VccQ/2; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(AC) Max, VSEH(AC) Min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 60. Single-Ended Levels for RE_t, RE_c, DQS_t, DQS_C (1.8V V_{CCQ})

Parameter	Symbol	Min	Max	Unit	Notes
Single-Ended high level	$V_{SEH(AC)}$	V_{CCQ}/2 + 0.250	see note	V	1
Single-Ended low level	$V_{SEL(AC)}$	See note	V_{CCQ}/2 + 0.250	V	1

Note: 1. These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.

Table 61. Differential AC Input/Output Parameters

Parameter	Symbol	Min	Max	Unit	Notes
AC differential input cross-point voltage relative to V_{CCQ} / 2	$V_{IX(AC)}$	0.5 x V_{CCQ} - 0.175	0.5 x V_{CCQ} - 0.175	V	1
AC differential output cross-point voltage	$V_{OX(AC)}$	0.5 x V_{CCQ} - 0.2	0.5 x V_{CCQ} + 0.2	V	2,3,4

Notes:
1. The typical value of $V_{IX(AC)}$ is expected to be 0.5 x V_{CCQ} of the transmitting device. $V_{IX(AC)}$ is expected to track variations in VCCQ. VIX(AC) indicates the voltage at which differential input signals shall cross.
2. The typical value of $V_{OX(AC)}$ is expected to be 0.5 x V_{CCQ} of the transmitting device. $V_{OX(AC)}$ is expected to track variations in V_{CCQ}. VOX(AC) indicates the voltage at which differential input signals shall cross.
3. VOX(AC) is measured with ½ DQ signals per data byte driving logic HIGH and ½ DQ signals per data byte driving logic LOW.
4. VOX(AC) is verified by design and characterization; it may not be subject to production testing.

Table 62. Asynchronous AC Characteristics: Command, Data, and Address Input

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		100		50		35		30		25		20		ns	
Frequency		≈ 10		≈ 20		≈ 28		≈ 33		≈ 40		≈ 50		MHz	
ALE to data start	^{t}ADL	200	–	100	–	100	–	100	–	70	–	70	–	ns	1
ALE hold time	^{t}ALH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
ALE setup time	^{t}ALS	50	–	25	–	15	–	10	–	10	–	10	–	ns	
ALE to RE# delay	^{t}AR	25	–	10	–	10	–	10	–	10	–	10	–	ns	
CE# access time	^{t}CEA	–	100	–	45	–	30	–	25	–	25	–	25	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	^{t}CEH	20	–	20	–	20	–	20	–	20	–	20	–	ns	
CE# hold time	^{t}CH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
CE# high to output high-Z	^{t}CHZ	–	100	–	50	–	50	–	50	–	30	–	30	ns	2

Table 62. Asynchronous AC Characteristics: Command, Data, and Address Input

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLE hold time	tCLH	20	–	10	–	10	–	5	–	5	–	5	–	ns	
CLE to RE# delay	tCLR	20	–	10	–	10	–	10	–	10	–	10	–	ns	
CLE setup time	tCLS	50	–	25	–	15	–	10	–	10	–	10	–	ns	
CE# high to output hold	tCOH	0	–	15	–	15	–	15	–	15	–	15	–	ns	
CE# setup time	tCS	70	–	35	–	25	–	25	–	20	–	15	–	ns	
Data hold time	tDH	20	–	10	–	5	–	5	–	5	–	5	–	ns	
Data setup time	tDS	40	–	20	–	15	–	10	–	10	–	7	–	ns	
ENi LOW until any issued command is ignored	tENI	-	15	-	15	-	15	-	15	-	15	-	15	ns	
CE_# LOW until ENo Low	tENo	-	50	-	50	-	50	-	50	-	50	-	50	ns	
Output High-Z to RE# low	tIR	10	–	0	–	0	–	0	–	0	–	0	–	ns	
RE# cycle time	tRC	100	–	50	–	35	–	30	–	25	–	20	–	ns	
RE# access time	tREA	–	40	–	30	–	25	–	20	–	20	–	16	ns	3
RE# high hold time	tREH	30	–	15	–	15	–	10	–	10	–	7	–	ns	3
RE# high to output hold	tRHOH	0	–	15	–	15	–	15	–	15	–	15	–	ns	3
RE# high to WE# low	tRHW	200	–	100	–	100	–	100	–	100	–	100	–	ns	
RE# high to output high-Z	tRHZ	–	200	–	100	–	100	–	100	–	100	–	100	ns	2, 3
RE# low to output hold	tRLOH	0	–	0	–	0	–	0	–	5	–	5	–	ns	3
RE# pulse width	tRP	50	–	25	–	17	–	15	–	12	–	10	–	ns	
Ready to RE# low	tRR	40	–	20	–	20	–	20	–	20	–	20	–	ns	
WE# high to R/B low	tWB	–	200	–	100	–	100	–	100	–	100	–	100	ns	4
WE# cycle time	tWC	100	–	45	–	35	–	30	–	25	–	20	–	ns	
WE# high hold time	tWH	30	–	15	–	15	–	10	–	10	–	7	–	ns	
WE# high to RE# low	tWHR	120	–	80	–	80	–	60	–	60	–	60	–	ns	
WE# pulse width	tWP	50	–	25	–	17	–	15	–	12	–	10	–	ns	
WP# transition to RE# low	tWW	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a Volume is selected	tVDLY	-	50	-	50	-	50	-	50	-	50	-	50	ns	

Notes:

1. Timing for tADL begins in the address cycle, on the final rising edge of WE# and ends with the first rising edge of WE# for data input.
2. Data transition is measured ±200mV from steady-steady voltage with load. This parameter is sampled and not 100 percent tested.
3. AC characteristics may need to be relaxed if output drive strength is not set to at least nominal.
4. Do not issue a new command during tWB, even if R/B# or RDY is ready.

32.0 Electrical Specifications — AC Characteristics and Operating Conditions (Onfi 2.3 and Onfi 3.0)

Table 63. AC Characteristics: Onfi 2.3 Command, Data, and Address Input

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		50		30		20		15		12		10		ns	
Frequency		≈20		≈ 33		≈ 50		≈67		≈ 83		≈100		MHz	
Access window of DQ[7:0] from CLK	tAC	3	20	3	20	3	20	3	20	3	20	3	20	ns	
ALE to data loading time	tADL	100	–	100	–	70	–	70	–	70	–	70	–	ns	
Command, address data delay	tCAD	25	-	25	-	25	-	25	-	25	-	25	-	ns	1
DQ hold — command, address	tCAH	10	-	5	-	4	-	3	-	2.5	-	2	-	ns	
ALE, CLE, W/R# hold	tCALH	10	-	5	-	4	-	3	-	2.5	-	2	-	ns	
ALE, CLE, W/R# setup	tCALS	10	-	5	-	4	-	3	-	2.5	-	2	-	ns	
DQ setup — command, address	tCAS	10	-	5	-	4	-	3	-	2.5	-	2	-	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	tCEH	20	-	20	-	20	-	20	-	20	-	20	-	ns	
CE# hold	tCH	10	-	5	-	4	-	3	-	2.5	-	2	-	ns	
Average CLK cycle time	tCK (avg)	50	100	30	50	20	30	15	20	12	15	10	12	ns	2
Absolute CLK cycle time, from rising edge to rising edge	tCK (abs)	tCK (abs) MIN = tCK (avg) + tJIT (per) MIN tCK (abs) MAX = tCK (avg) + tJIT (per) MAX												ns	
CLK cycle HIGH	tCKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK	3
CLK cycle LOW	tCKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK	3
Data output end to W/R# HIGH	tCKWR	tCKWR(MIN) = RoundUp[(tDQSCK(MAX) + tCK)/tCK]												tCK	
CE# setup	tCS	35	-	25	-	15	-	15	-	15	-	15	-	ns	
Data in hold	tDH	5	-	2.5	-	1.7	-	1.3	-	1.1	-	0.9	-	ns	
Access window of DQS from CLK	tDQSCK	-	20	-	20	-	20	-	20	-	20	-	20	ns	
DQS, DQ[7:0] Driven by NAND	tDQSD	-	18	-	18	-	18	-	18	-	18	-	18	ns	
DQS, DQ[7:0] to tri-state	tDQSHZ	-	20	-	20	-	20	-	20	-	20	-	20	ns	4

Table 63. AC Characteristics: Onfi 2.3 Command, Data, and Address Input (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS input high pulse width	^{t}DQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS input low pulse width	^{t}DQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-DQ skew	^{t}DQSQ	-	5	-	2.5	-	1.7	-	1.3	-	1.0	-	0.85	ns	
Data input	^{t}DQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
Data in setup	^{t}DS	5	-	3	-	2	-	1.5	-	1.1	-	0.9	-	ns	
DQS falling edge from CLK rising — hold	^{t}DSH	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK	
DQS falling to CLK rising — set-up	^{t}DSS	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	tCK	
Data valid window	^{t}DVW	^{t}DVW = ^{t}QH = ^{t}DQSQ													
ENi LOW until any issued command is ignored	^{t}ENi	-	15	-	15	-	15	-	15	-	15	-	15	ns	
CE_# LOW until ENo LOW	^{t}ENo	-	50	-	50	-	50	-	50	-	50	-	50	ns	
Half clock period	^{t}HP	^{t}HP = Min(^{t}CKH, ^{t}CKL)												ns	
The deviation of a given ^{t}CK (abs) from a ^{t}CK (avg)	^{t}JIT (per)	-0.7	0.7	-0.7	0.7	-0.7	0.7	-0.6	0.6	-0.6	0.6	-0.5	0.5	ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^{t}QH	^{t}QH = ^{t}HP - ^{t}QHS												ns	
Data hold skew factor	^{t}QHS	-	6	-	3	-	2	-	1.5	-	1.2	-	1	ns	
Data output to command, address, or data input	^{t}RHW	100	-	100	-	100	-	100	-	100	-	100	-	ns	
Ready to data output	^{t}RR	20	-	20	-	20	-	20	-	20	-	20	-	ns	
CLK HIGH to R/B# LOW	^{t}WB	-	100	-	100	-	100	-	100	-	100	-	100	ns	
Command cycle to data output	^{t}WHR	80	-	80	-	80	-	80	-	80	-	80	-	ns	
DQS write preamble	^{t}WPRE	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	^{t}CK	
DQS write post-preamble	^{t}WPST	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	^{t}CK	

Table 63. AC Characteristics: Onfi 2.3 Command, Data, and Address Input (Continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
W/R# LOW to data output cycle	tWRCK	20	-	20	-	20	-	20	-	20	-	20	-	ns	
WP# transition to command cycle	tWW	100	-	100	-	100	-	100	-	100	-	100	-	ns	
Delay before next command after a Volume is selected	tVDLY	-	50	-	50	-	50	-	50	-	50	-	50	ns	

Notes:
1. Delay is from start of command to next command, address, or data cycle; start of address to next command, address, or data cycle; and end of data to start of next command, address, or data cycle.
2. tCK(avg) is the average clock period over any consecutive 200-cycle window.
3. tCKH(abs) and tCKL(abs) include static offset and duty cycle jitter.
4. tDQSHZ begins when W/R# is latched HIGH by CLK. This parameter is not referenced to a specific voltage level; it specifies when the device outputs are no longer driving.
5. If RESET (FFh) is issued when the target is idle, the target goes busy for a maximum of 5µs.

Table 64. AC Characteristics: Onfi 3.0 Command, Data, and Address for modes 0-4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		30		25		15		12		10		ns	
Frequency		≈33		≈ 40		≈ 66		≈83		≈ 100		MHz	
Command and Address													
Access window of DQ[7:0] from RE# LOW or RE_t/RE_c	tAC	3	25	3	25	3	25	3	25	3	25	ns	
ALE to data loading time	tADL	100	–	100	–	100	–	100	–	70	–	ns	
ALE to RE# LOW or RE_t/ RE_c	tAR	10	-	10	-	10	-	10	-	10	-	ns	
DQ hold — command, address	tCAH	5	-	5	-	5	-	5	-	5	-	ns	
ALE, CLE hold	tCALH	5	-	5	-	5	-	5	-	5	-	ns	
ALE, CLE setup with ODT disabled	tCALS	15	-	15	-	15	-	15	-	15	-	ns	
ALE, CLE setup with ODT enabled	tCALS	15	-	15	-	15	-	15	-	15	-	ns	
DQ setup — command, address	tCAS	5	-	5	-	5	-	5	-	5	-	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	tCEH	20	-	20	-	20	-	20	-	20	-	ns	
CE# hold	tCH	5	-	5	-	5	-	5	-	5	-	ns	
CE# HIGH to output Hi-Z	tCHZ	-	30	-	30	-	30	-	30	-	30	ns	1
CLE HIGH to output Hi-Z	tCLHZ	-	30	-	30	-	30	-	30	-	30		1
CLE to RE# LOW or RE_t/ RE_c	tCLR	10	-	10	-	10	-	10	-	10	-	ns	
CE to RE# LOW or RE_t/RE_c	tCR	10	-	10	-	10	-	10	-	10	-	ns	

Table 64. AC Characteristics: Onfi 3.0 Command, Data, and Address for modes 0-4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CE# setup	tCS	20	-	20	-	20	-	20	-	20	-	ns	
CE# setup for data output with ODT disabled	tCS1	30	-	30	-	30	-	30	-	30	-	ns	
CE# setup for DQS/DQ[7:0] with ODT disabled	tCS2	40	-	40	-	40	-	40	-	40	-	ns	
ALE, CLE, WE# hold time from CE# HIGH	tCSD	10	-	10	-	10	-	10	-	10	-	ns	
ENi LOW until any issued command is ignored	tENi	-	15	-	15	-	15	-	15	-	15	ns	
CE_# LOW until ENo LOW	tENo	-	50	-	50	-	50	-	50	-	50	ns	
Ready to data output	tRR	20	-	20	-	20	-	20	-	20	-	ns	
CLK HIGH to R/B# LOW	tWB	-	100	-	100	-	100	-	100	-	100	ns	
WE# cycle time	tWC	25	-	25	-	25	-	25	-	25	-	ns	
Command cycle to data output	tWHR	80	-	80	-	80	-	80	-	80	-	ns	
WP# transition to command cycle	tWP	11	-	11	-	11	-	11	-	11	-	ns	
WP# transition to command cycle	tWW	100	-	100	-	100	-	100	-	100	-	ns	
Delay before next command after a Volume is selected	tVDLY	-	50	-	50	-	50	-	50	-	50	ns	
Jitter													
The deviation of a given tDQS (abs) / tDSC (abs) from a tDQS (avg) / tDSC (avg)	tJITper (DQS)	-2.4	2.4	-2.0	2.0	-1.2	1.2	-1.0	1.0	-0.8	0.8	ns	3,5,7
The deviation of a given tRC (abs) / tDSC (abs) from a tRC (avg) / tDSC (avg)	tJITper (RE#)	-1.8	1.8	-1.5	1.5	-0.9	0.9	-0.75	0.75	-0.6	0.6	ns	3,5,7
Cycle to cycle jitter for DQS	tJITcc (DQS)	4.8	-	4.0	-	2.4	-	2.0	-	1.6	-	ns	3,6
Cycle to cycle jitter for RE#	tJITcc (RE#)	3.6	-	3.0	-	1.8	-	1.5	-	1.2	-	ns	3,6
Data Input													
DQS setup time for data input start	tCDQSS	30	-	30	-	30	-	30	-	30	-	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	tDBS	5	-	5	-	5	-	5	-	5	-	ns	
Data in hold	tDH	4.0	-	3.3	-	2.0	-	1.1	-	0.7	-	ns	10
Data in setup	tDS	4.0	-	3.3	-	2.0	-	1.1	-	0.7	-	ns	10
DQS input high pulse width	tDQSH	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	tDSC (avg)	
DQS input low pulse width	tDQSL	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	tDSC (avg)	
Average DQS cycle time	tDSC (avg) or tDSC	30	-	25	-	15	-	12	-	10	-	ns	2

Table 64. AC Characteristics: Onfi 3.0 Command, Data, and Address for modes 0-4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Absolute DQS cycle time, from rising edge to rising edge	tDSC	tDSC (abs) MIN = tDSC (avg) + tJITper(DQS) MIN tDSC (abs) MAX = tDSC (avg) + tJITper(DQS) MAX				tDSC (abs) MIN = tDSC (avg) + tJITper(DQS) MIN tDSC (abs) MAX = tDSC (avg) + tJITper(DQS) MAX							
ENi LOW until any issued command is ignored	tENi	-	15	-	15	-	15	-	15	-	15	ns	
CE_# LOW until ENo LOW	tEN0	-	50	-	50	-	50	-	50	-	50	ns	
DQS write preable with ODT disabled	tWPRE	15	-	15	-	15	-	15	-	15	-	ns	
DQS write preable with ODT enabled	tWPRE2	25	-	25	-	25	-	25	-	25	-	ns	
DQS write post-amble	tWPST	6.5	-	6.5	-	6.5	-	6.5	-	6.5	-	ns	
DQS write post-amble hold time	tWPSTH	5	-	5	-	5	-	5	-	5	-	ns	
Data Output													
Access window of DQ[7:0] from CLK	tAC	3	25	3	25	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	tDBS	5	-	5	-	5	-	5	-	5	-	ns	
DQS-DQ skew	tDQSQ	5	18	5	18	5	18	5	18	5	18	ns	
Access window of DQS from RE# or RE_t / RE_c	tDQSRE	3	25	3	25	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	tDQSD	5	18	5	18	5	18	5	18	5	18	ns	
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	tDQSRH	5	-	5	-	5	-	5	-	5	-	ns	
Data valid window	tDVW	tDVW = tQH - tDQSQ								tDVW = tQH - tDQSQ		ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	tQH	0.37	-	0.37	-	0.37	-	0.37	-	0.37	-	tRC (avg)	9
DQS (DQS_t /DQS_c) output HIGH time	tQSH	0.37	-	0.37	-	0.37	-	0.37	-	0.37	-	tRC (avg)	9
DQS (DQS_t / DQS_c) output LOW time	tQSL	0.37	-	0.37	-	0.37	-	0.37	-	0.37	-	tRC (avg)	9
Average RE# cycle time	tRC (avg) or tRC	30	-	25	-	15	-	12	-	10	-	ns	2
Absolute RE# cycle time	tRC (abs)	tRC (abs) MIN = tRC (avg) +tJITper(RE#) MIN								tRC (abs) MIN = tRC (avg) +tJITper(RE#) MIN		ns	

Table 64. AC Characteristics: Onfi 3.0 Command, Data, and Address for modes 0-4

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Average RE# HIGH hold time	^{t}REH (avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Absolute RE# HIGH hold time	^{t}REH (abs)	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	^{t}RC (avg)	4
Data output to command, address, or data input	^{t}RHW (avg)	100	-	100	-	100	-	100	-	100	-	ns	
Average RE# pulse width	^{t}RP (avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Average RE# pulse width	^{t}RP (avg)	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	^{t}RC (avg)	4
Absolute RE# pulse width	^{t}RP (abs)	0.43		0.43		0.43	-	0.43	-	0.43	-	^{t}RC (avg)	
Read preamble with ODT disabled	^{t}RPE	15	-	15	-	15	-	15	-	15	-	ns	
Read preamble with ODT enabled	^{t}RPE2	25	-	25	-	25	-	25	-	25	-	ns	
Read postamble	^{t}RPST	^{t}DQSRE + 0.5 * ^{t}RC	-	^{t}DQSRE + 0.5 * ^{t}RC	-	^{t}DQSRE + 0.5 * ^{t}RC	-	^{t}DQSRE + 0.5 * ^{t}RC	-	^{t}DQSRE + 0.5 * ^{t}RC	-	ns	
Read postamble hold time	^{t}RPSTH	5	-	5	-	5	-	5	-	5	-	ns	

Notes:
1. tCHZ and tCLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.
2. The parameters tRC(avg) and tDSC(avg) are the average over any 200 consecutive periods and tRC(avg) / tDSC(avg) min are the smallest rates allowed, with the exception of a deviation due to tJIT (per).
3. Input jitter is allowed provided it does not exceed values specified.
4. tREH(avg) and tRP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter tJIT (per) is the maximum deviation in the tRC or tDSC period from the average or nominal tRC or tDSC period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter tJITcc is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed tJITper. As long as the absolute minimum half period (tRP(abs), tREH(abs), tDQSH or tDQSL is not less than 43 percent of the average cycle.
8. All timing parameter values assume differential signaling for RE# and DQS is used.
9. When the device is operated with input clock jitter, tQSL, tQSH, and tQH need to be derated by the actual tJITper in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
10. The tDS and tDH times listed are based on an input slew rate of 1 V/ns. If the input slew rate is not 1 V/ns, then the derating methodology shall be used.

Table 65. AC Characteristics: Onfi 3.0 Command, Data, and Address for modes 5-7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Note
		Min	Max	Min	Max	Min	Max		
Clock period		7.5		6		5		ns	
Frequency		≈133		≈ 166		≈ 200		MHz	
Command and Address									
Access window of DQ[7:0] from RE# LOW or RE_t/RE_c	^{t}AC	3	25	3	25	3	25	ns	

Table 65. AC Characteristics: Onfi 3.0 Command, Data, and Address for modes 5-7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Note
		Min	Max	Min	Max	Min	Max		
ALE to data loading time	tADL	70	–	70	–	70	–	ns	
ALE to RE# LOW or RE_t/RE_c	tAR	10	-	10	-	10	-	ns	
DQ hold — command, address	tCAH	5	-	5	-	5	-	ns	
ALE, CLE hold	tCALH	5	-	5	-	5	-	ns	
ALE, CLE setup with ODT disabled	tCALS	15	-	15	-	15	-	ns	
ALE, CLE setup with ODT enabled	tCALS	25	-	25	-	25	-	ns	
DQ setup — command, address	tCAS	5	-	5	-	5	-	ns	
CE# HIGH hold time	tCEH	20	-	20	-	20	-	ns	
CE# hold	tCH	5	-	5	-	5	-	ns	
CE# HIGH to output Hi-Z	tCHZ	-	30	-	30	-	30	ns	1
CLE HIGH to output Hi-Z	tCLHZ	-	30	-	30	-	30		1
CLE to RE# LOW or RE_t/RE_c	tCLR	10	-	10	-	10	-	ns	
CE to RE# LOW or RE_t/RE_c	tCR	10	-	10	-	10	-	ns	
CE# setup	tCS	20	-	20	-	20	-	ns	
CE# setup for data output with ODT disabled	tCS1	30	-	30	-	30	-	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	tCS2	40	-	40	-	40	-	ns	
ALE, CLE, WE# hold time from CE# HIGH	tCSD	10	-	10	-	10	-	ns	
ENi LOW until any issued command is ignored	tENi	-	15	-	15	-	15	ns	
CE_# LOW until ENo LOW	tENo	-	50	-	50	-	50	ns	
Ready to data output	tRR	20	-	20	-	20	-	ns	
CLK HIGH to R/B# LOW	tWB	-	100	-	100	-	100	ns	
WE# cycle time	tWC	25	-	25	-	25	-	ns	
Command cycle to data output	tWHR	80	-	80	-	80	-	ns	
WP# transition to command cycle	tWP	11	-	11	-	11	-	ns	
WP# transition to command cycle	tWW	100	-	100	-	100	-	ns	
Delay before next command after a Volume is selected	tVDLY	-	50	-	50	-	50	ns	
Jitter									
The deviation of a given tDQS (abs) / tDSC (abs) from a tDQS (avg) / tDSC (avg)	tJITper (DQS)	-0.6	0.6	-0.48	0.48	-0.40	0.40	ns	3,5,7
The deviation of a given tRC (abs) / tDSC (abs) from a tRC (avg) / tDSC (avg)	tJITper (RE#)	-0.45	0.45	-0.36	0.36	-0.30	0.30	ns	3,5,7
Cycle to cycle jitter for DQS	tJITcc (DQS)	1.2	-	0.96	-	0.80	-	ns	3,6
Cycle to cycle jitter for RE#	tJITcc (RE#)	0.9	-	0.72	-	0.60	-	ns	3,6
Data Input									
DQS setup time for data input start	tCDQSS	30	-	30	-	30	-	ns	

Table 65. AC Characteristics: Onfi 3.0 Command, Data, and Address for modes 5-7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Note
		Min	Max	Min	Max	Min	Max		
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	^{t}DBS	5	-	5	-	5	-	ns	
Data in hold	^{t}DH	0.5	-	0.3	-	0.28	-	ns	10
Data in setup	^{t}DS	0.5	-	0.3	-	0.28	-	ns	10
DQS input high pulse width	^{t}DQSH	0.43	-	0.43	-	0.43	-	^{t}DSC (avg)	
DQS input low pulse width	^{t}DQSL	0.43	-	0.43	-	0.43	-	^{t}DSC (avg)	
Average DQS cycle time	^{t}DSC (avg) or ^{t}DSC	7.5	-	6	-	5	-	ns	2
Absolute DQS cycle time, from rising edge to rising edge	^{t}DSC (abs)	tDSC (abs) MIN = tDSC (avg) + tJITper(DQS) MIN tDSC (abs) MAX = tDSC (avg) + tJITper(DQS) MAX						ns	
ENi LOW until any issued command is ignored	^{t}ENi	-	15	-	15	-	15	ns	
CE_# LOW until ENo LOW	^{t}EN0	-	50	-	50	-	50	ns	
DQS write preamble with ODT disabled	^{t}WPRE	15	-	15	-	15	-	ns	
DQS write preamble with ODT enabled	^{t}WPRE2	25	-	25	-	25	-	ns	
DQS write post-amble	^{t}WPST	6.5	-	6.5	-	6.5	-	ns	
DQS write post-amble hold time	^{t}WPSTH	5	-	5	-	5	-	ns	
Data Output									
Access window of DQ[7:0] from CLK	^{t}AC	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	^{t}DBS	5	-	5	-	5	-	ns	
DQS-DQ skew	^{t}DQSQ	-	0.6	-	0.5	-	0.4	ns	
Access window of DQS from RE# or RE_t / RE_c	^{t}DQSRE	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	^{t}DQSD	5	18	5	18	5	18	ns	
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	^{t}DQSRH	5	-	5	-	5	-	ns	
Data valid window	^{t}DVW	^{t}DVW = ^{t}QH - ^{t}DQSQ						ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	^{t}QH	0.37	-	0.37	-	0.37	-	^{t}RC (avg)	9
DQS (DQS_t /DQS_c) output HIGH time	^{t}QSH	0.37	-	0.37	-	0.37	-	^{t}RC (avg)	9
DQS (DQS_t / DQS_c) output LOW time	^{t}QSL	0.37	-	0.37	-	0.37	-	^{t}RC (avg)	9
Average RE# cycle time	^{t}RC (avg) or ^{t}RC	7.5	-	6	-	5	-	ns	2
Absolute RE# cycle time	^{t}RC (abs)	^{t}RC (abs) MIN = ^{t}RC (avg) +^{t}JITper(RE#) MIN						ns	

Table 65. AC Characteristics: Onfi 3.0 Command, Data, and Address for modes 5-7 (Continued)

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Note
		Min	Max	Min	Max	Min	Max		
Average RE# HIGH hold time	tREH (avg)	0.45	0.55	0.45	0.55	0.45	0.55	tRC (avg)	4
Absolute RE# HIGH hold time	tREH (abs)	0.43	-	0.43	-	0.43	-	tRC (avg)	
Data output to command, address, or data input	tRHW (avg)	100	-	100	-	100	-	ns	
Average RE# pulse width	tRP (avg)	0.45	0.55	0.45	0.55	0.45	0.55	tRC (avg)	4
Absolute RE# pulse width	tRP (abs)	0.43		0.43		0.43	-	tRC (avg)	
Read preamble with ODT disabled	tRPRE	15	-	15	-	15	-	ns	
Read preamble with ODT enabled	tRPRE2	25	-	25	-	25	-	ns	
Read postamble	tRPST	tDQSRE + 0.5 * tRC	-	tDQSRE + 0.5 * tRC	-	tDQSRE + 0.5 * tRC	-	ns	
Read postamble hold time	tRPSTH	5	-	5	-	5	-	ns	

Notes:

1. tCHZ and tCLHZ are not referenced to a specific voltage level, but specify when the device output is no longer driving.
2. The parameters tRC(avg) and tDSC(avg) are the average over any 200 consecutive periods and tRC(avg) / tDSC(avg) min are the smallest rates allowed, with the exception of a deviation due to tJIT (per).
3. Input jitter is allowed provided it does not exceed values specified.
4. tREH(avg) and tRP(avg) are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
5. The period jitter tJIT (per) is the maximum deviation in the tRC or tDSC period from the average or nominal tRC or tDSC period. It is allowed in either the positive or negative direction.
6. The cycle-to-cycle jitter tJITcc is the amount the clock period can deviate from one cycle to the next.
7. The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed tJITper. As long as the absolute minimum half period (tRP(abs), tREH(abs), tDQSH or tDQSL is not less than 43 percent of the average cycle.
8. All timing parameter values assume differential signaling for RE# and DQS is used.
9. When the device is operated with input clock jitter, tQSL,tQSH, and tQH need to be derated by the actual tJITper in the input clock. (Output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
10. The tDS and tDH times listed are based on an input slew rate of 1 V/ns. If the input slew rate is not 1 V/ns, then the derating methodology shall be used.

33.0 Electrical Specifications — Array Characteristics

Table 67. MLC Array Characteristics

Symbol	Parameter	Typ	Max	Unit
NOP	Number of partial page programs	–	1	Cycles
^{t}BERS	ERASE BLOCK operation time	5	15	ms
^{t}CBSY	Cache busy	35	2500	µs
^{t}CCS	Change column setup time to data in/out or next command	200	-	ns
^{t}DBSY	Dummy busy time	0.5	1	µs
^{t}ESPD	ERASE SUSPEND operation time	-	1100	µs
^{t}ESPDN	ERASE SUSPEND operation time with no erase suspend	-	18	µs
^{t}RCBSY	Cache read busy time	3	150	µs
^{t}FEAT	Busy time for SET FEATURES and GET FEATURES operations	-	1	µs
^{t}ITC	Busy time interface change	-	1	µs
^{t}POR	Power-on reset time		1	ms
^{t}PROG	PAGE PROGRAM operation time	1250	3000	µs
^{t}R	READ PAGE operation time	65	110	µs
^{t}RST	Device reset time (Read/Program/Erase)	-	5/10/500	µs

34.0 Asynchronous Interface Timing Diagrams

Figure 83. RESET Operation

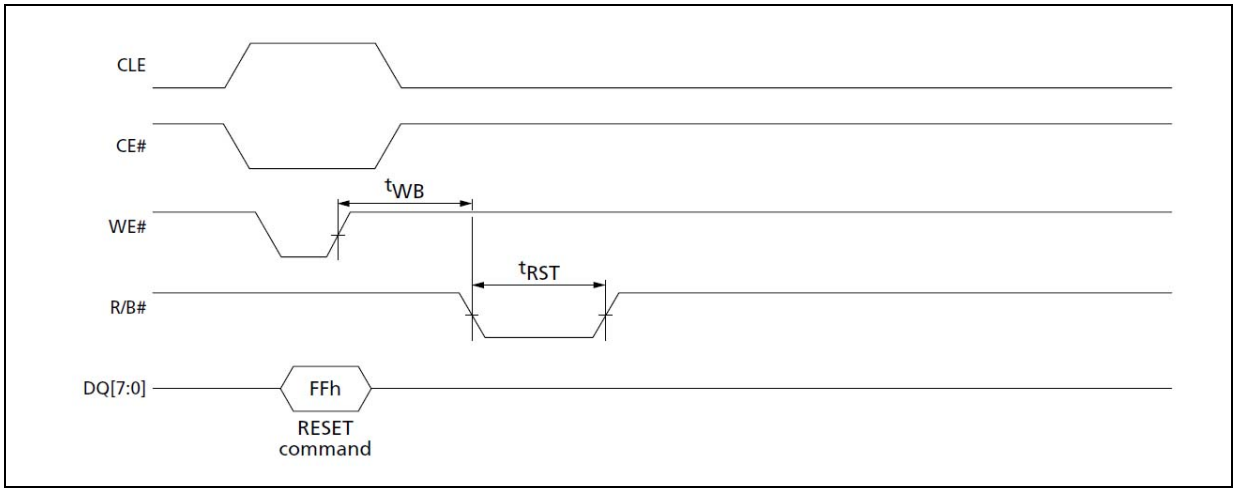


Figure 84. RESET LUN Operation

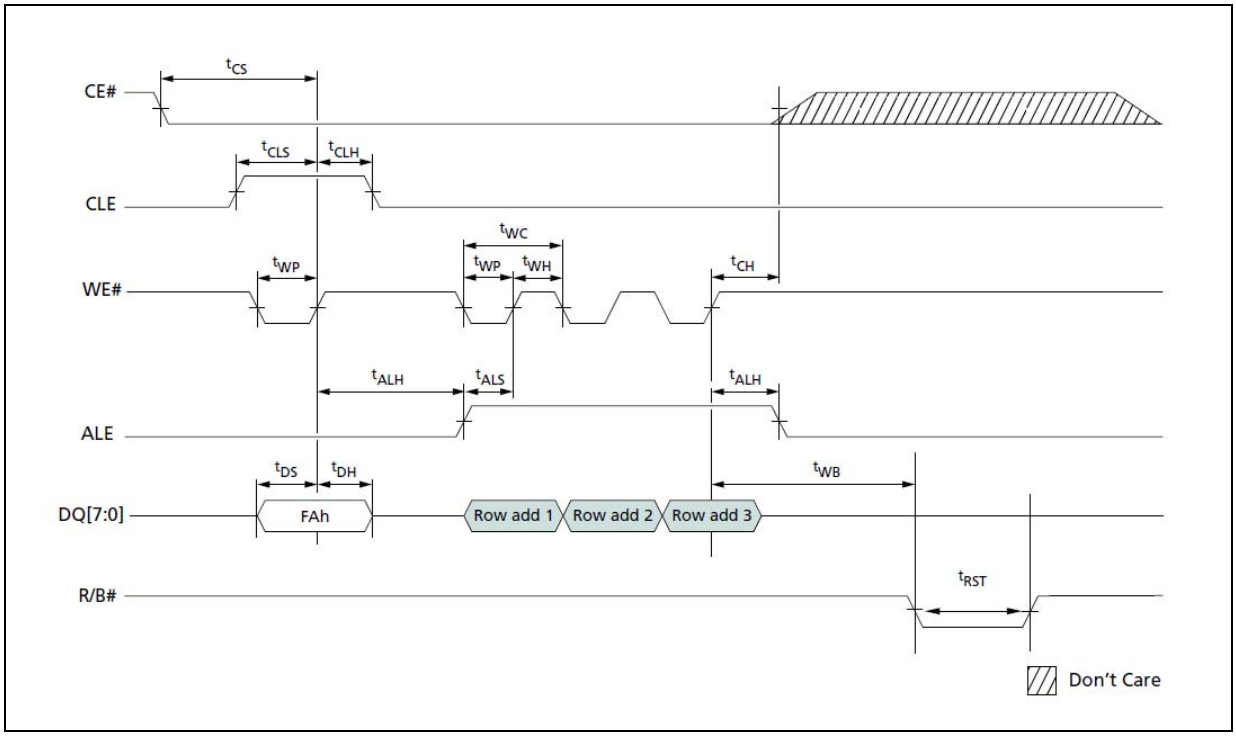


Figure 85. READ STATUS Cycle

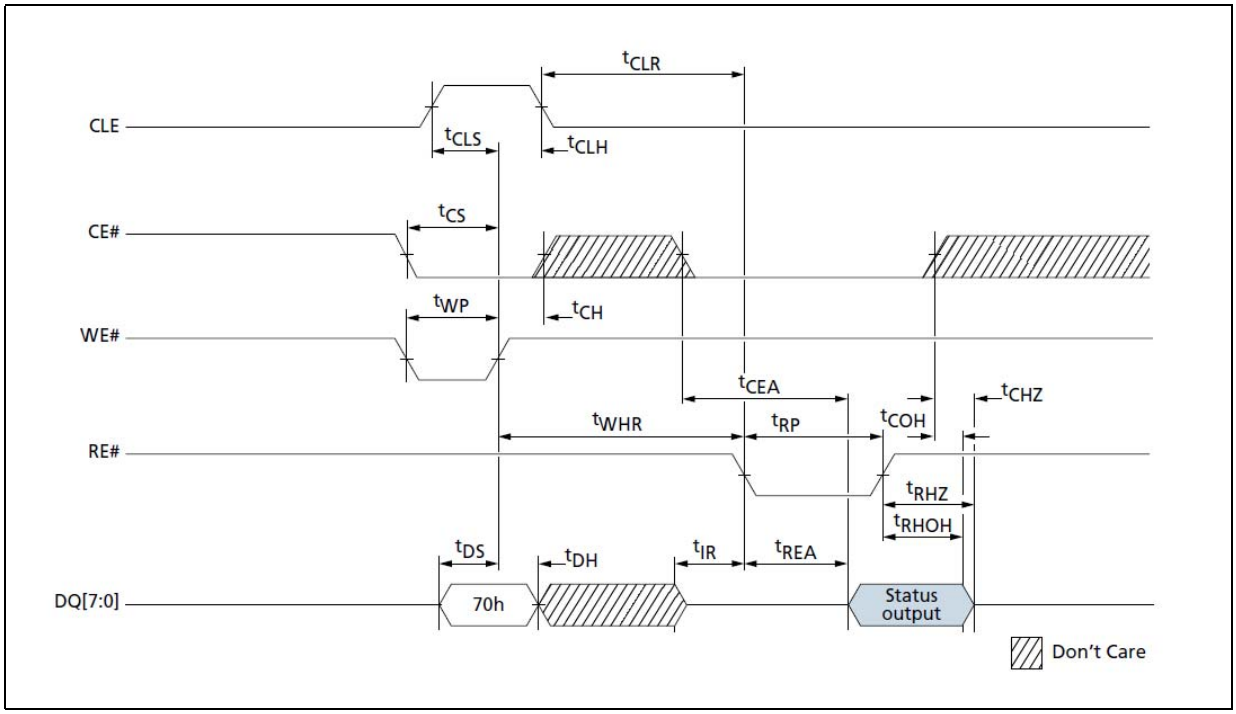


Figure 86. READ STATUS ENHANCED Cycle

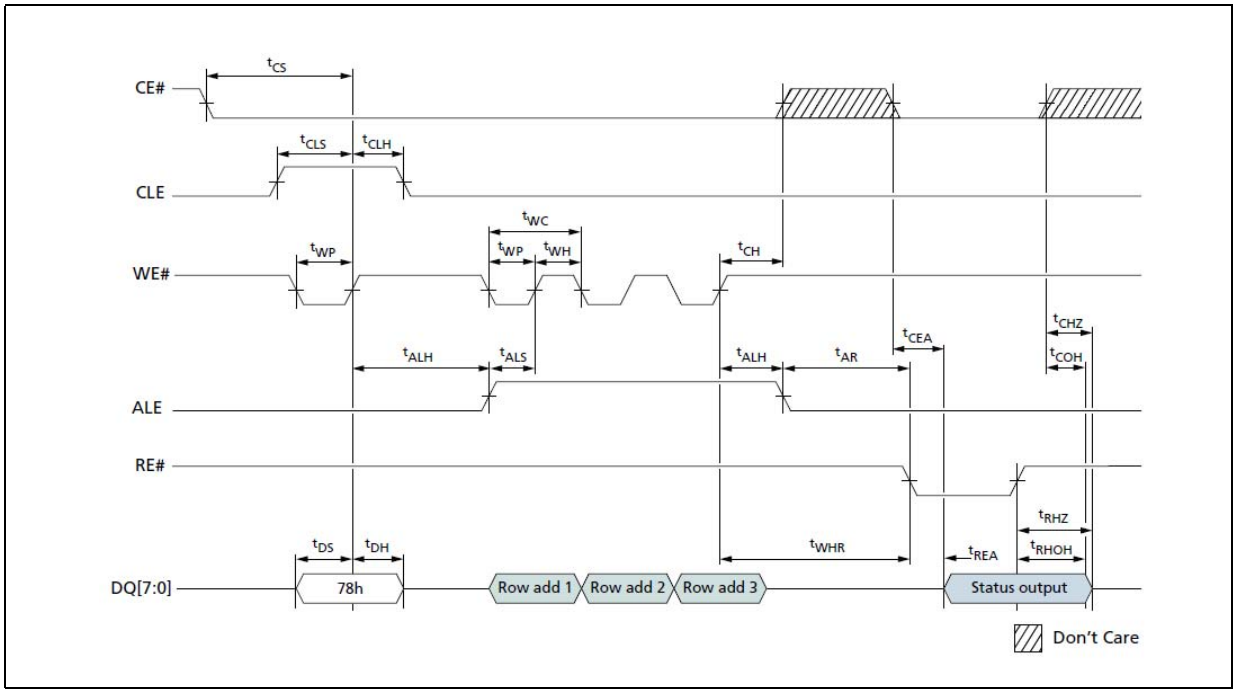


Figure 87. READ PARAMETER Page

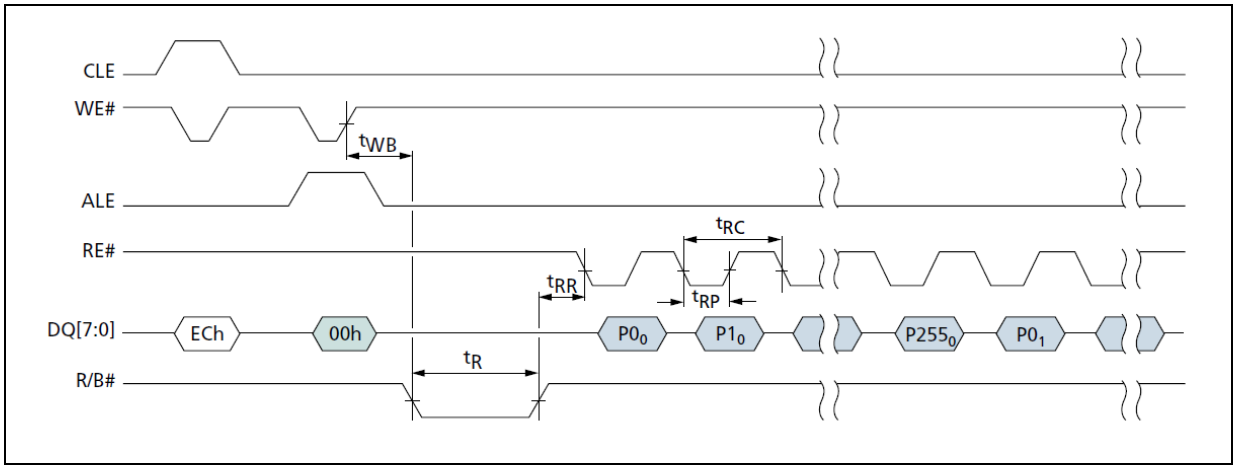


Figure 88. READ Page

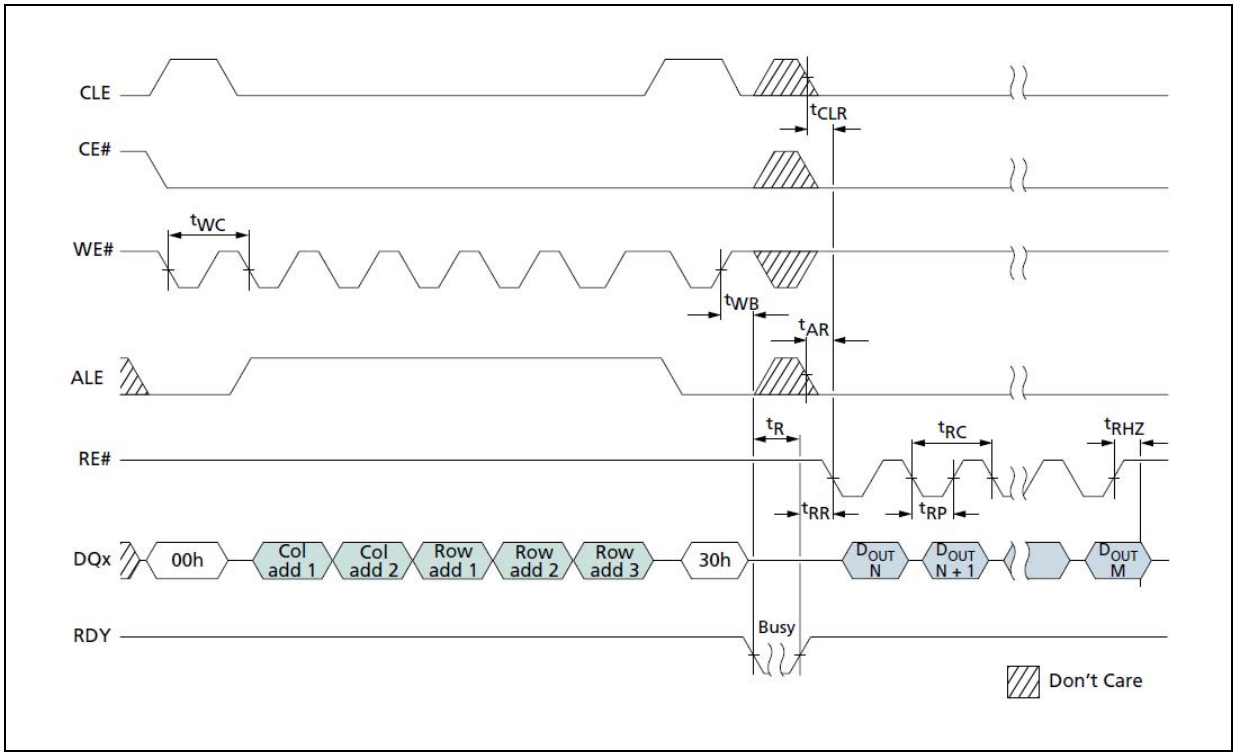


Figure 89. READ PAGE Operation with CE# "Don't Care"

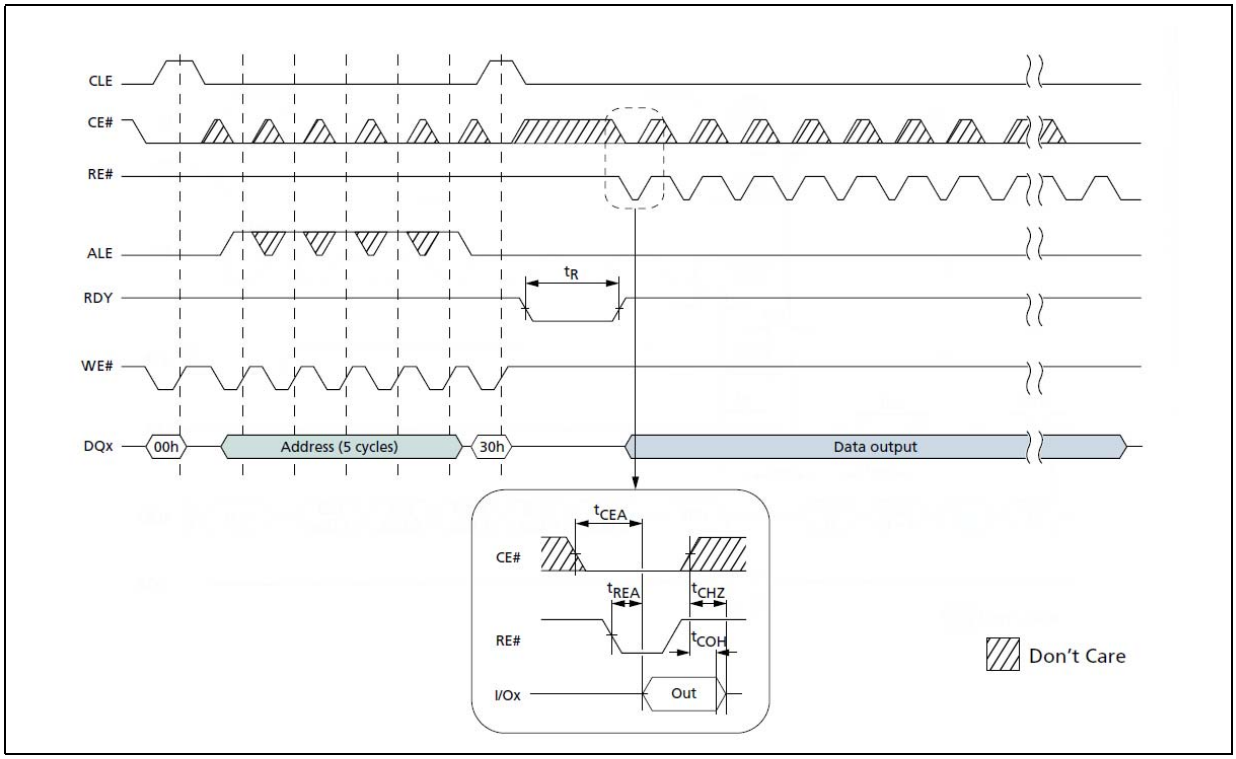


Figure 90. CHANGE READ Column

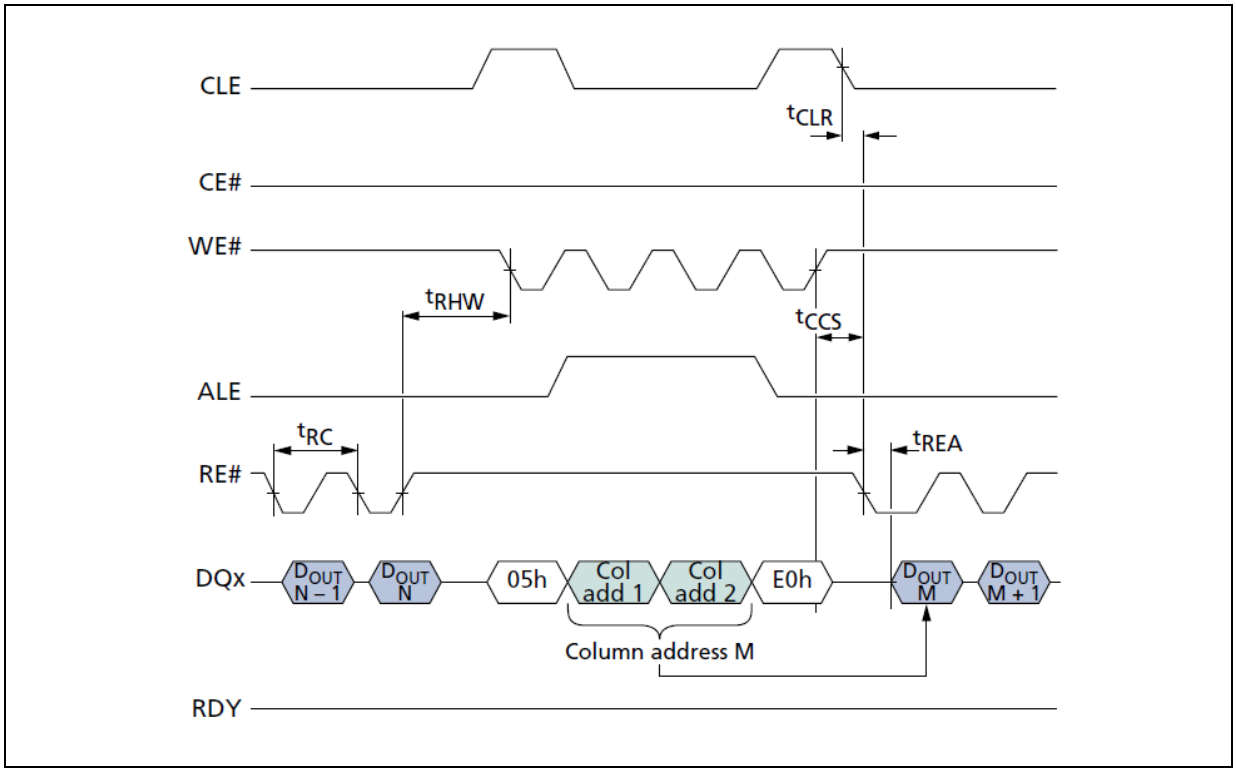


Figure 91. READ PAGE CACHE SEQUENTIAL

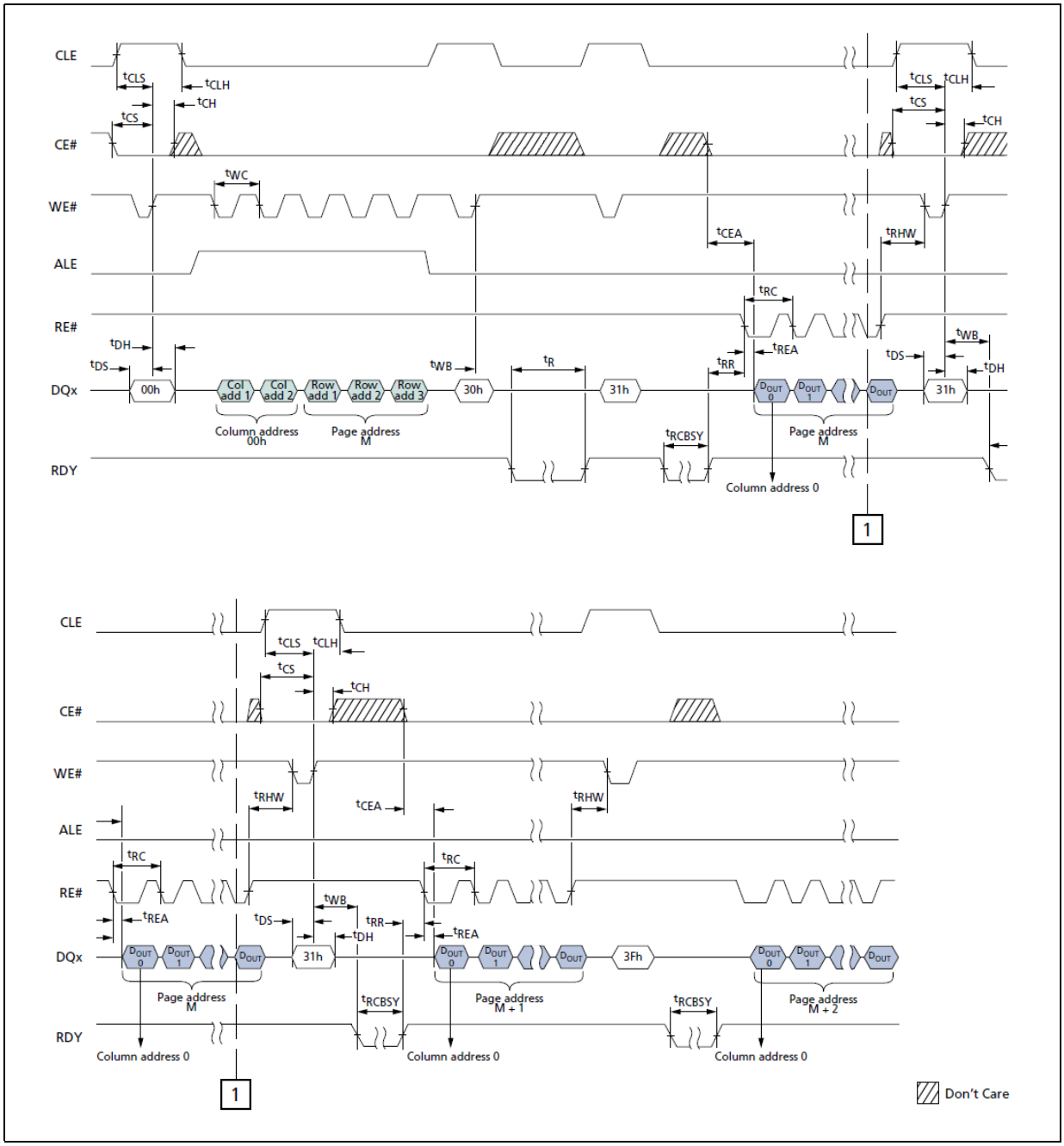


Figure 92. READ PAGE CACHE RANDOM

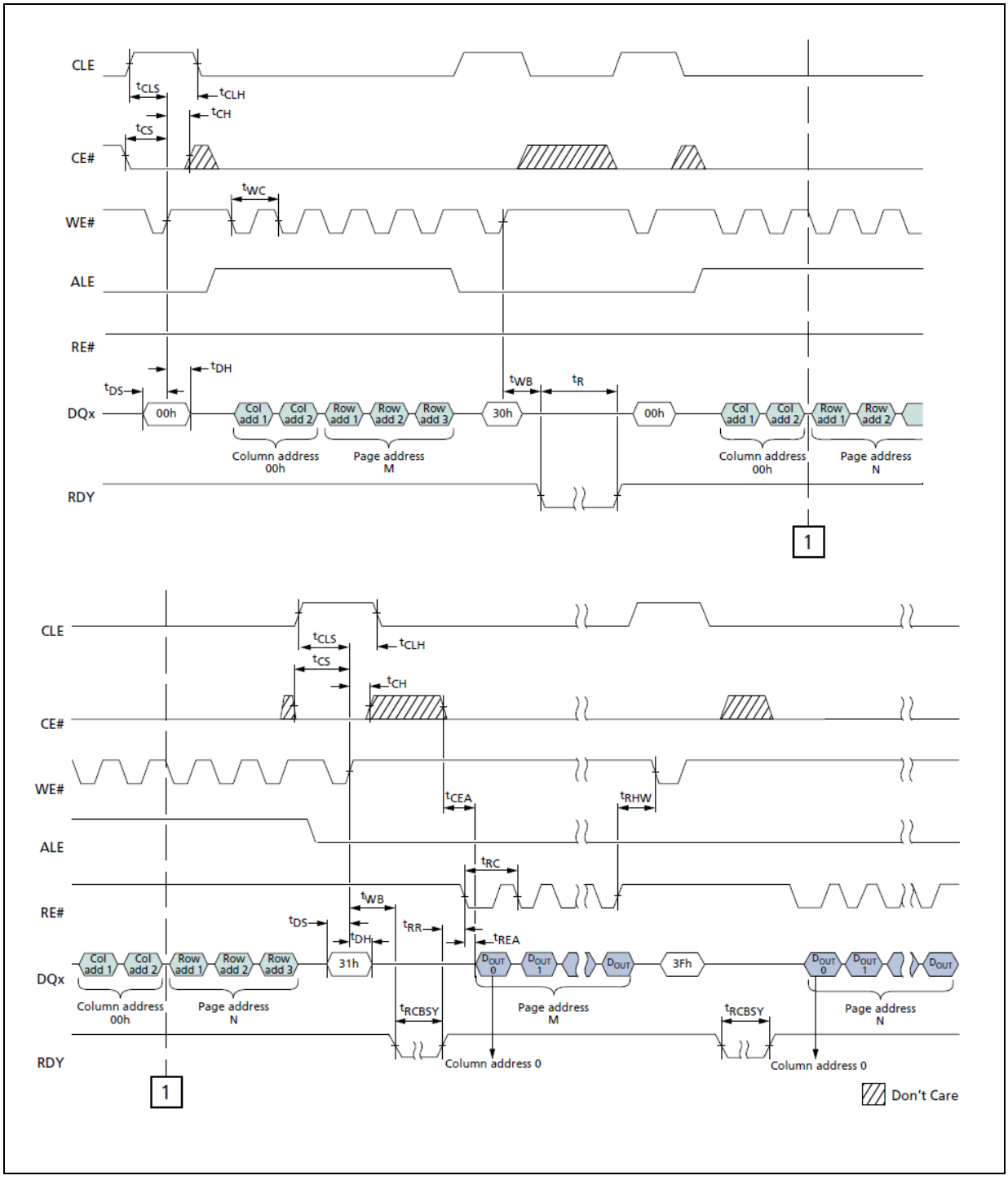


Figure 93. READ ID Operation

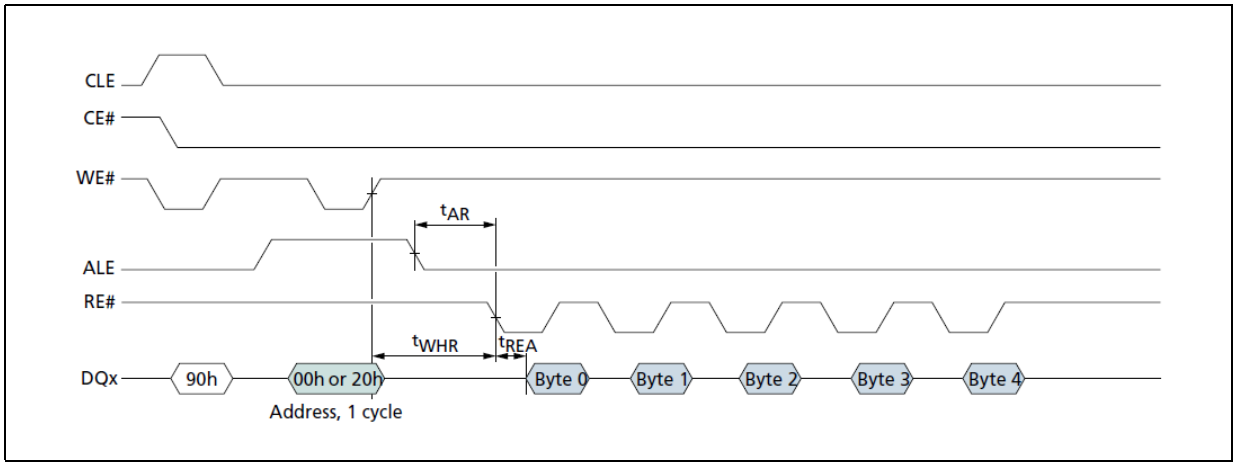


Figure 94. PROGRAM PAGE Operation

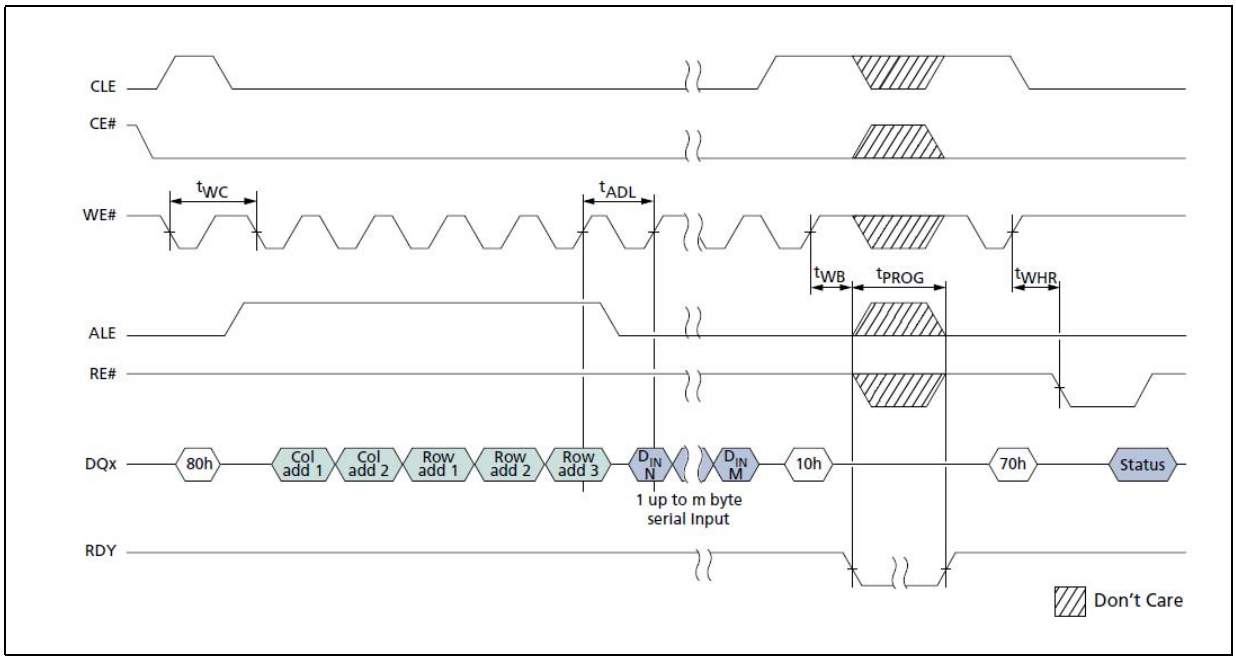


Figure 95. PROGRAM PAGE Operation with CE# "Don't Care"

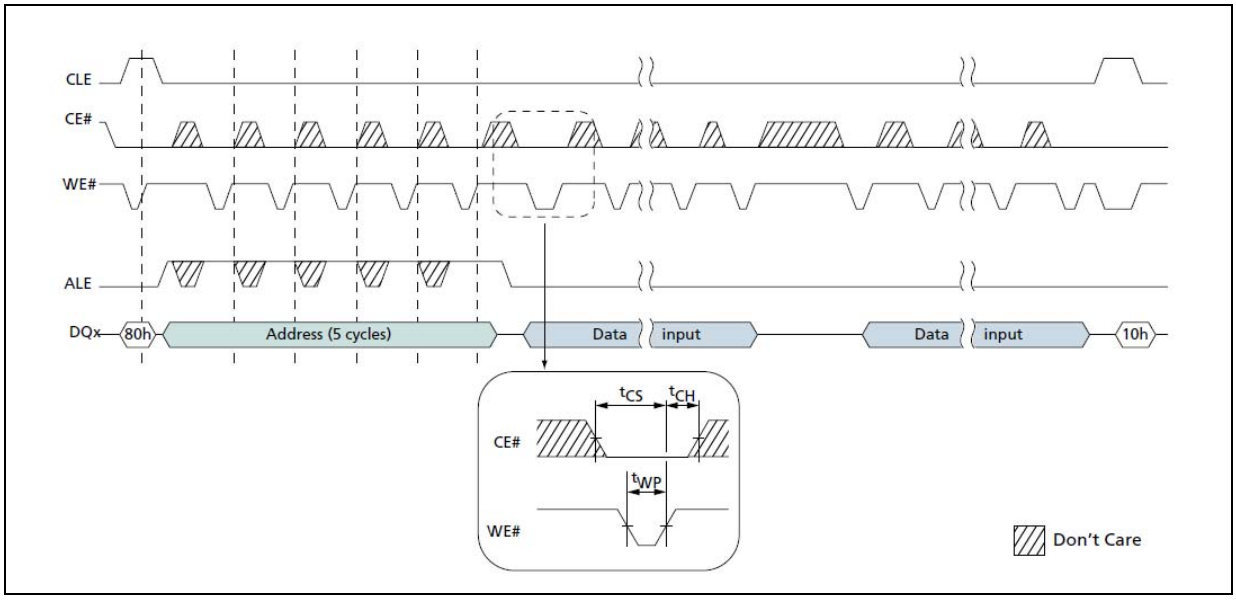


Figure 96. PROGRAM PAGE Operation with CHANGE WRITE COLUMN

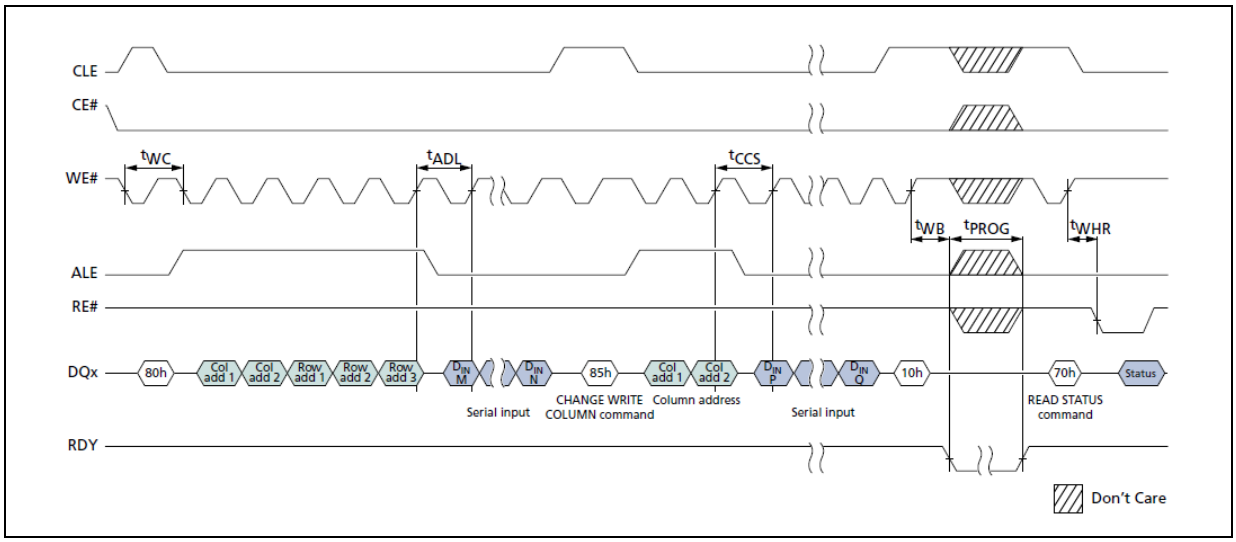


Figure 97. PROGRAM PAGE CACHE

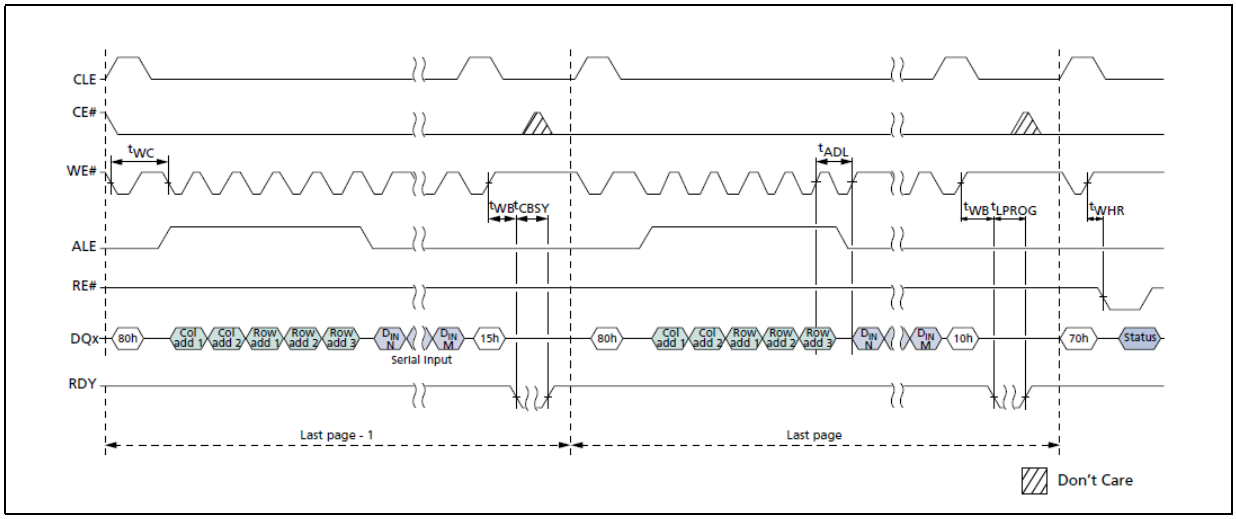


Figure 98. PROGRAM PAGE CACHE Ending on 15h

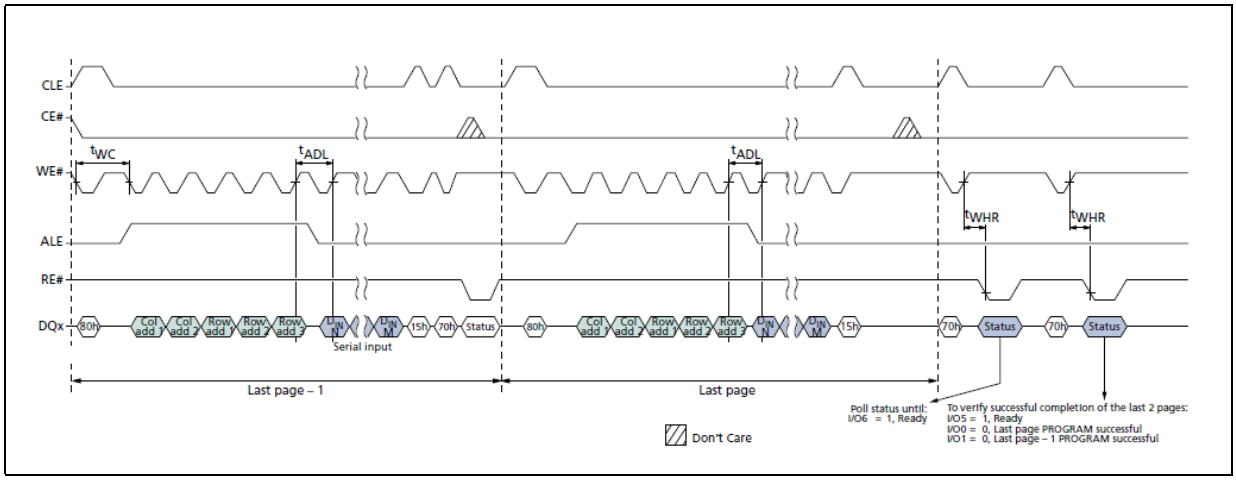


Figure 99. COPYBACK

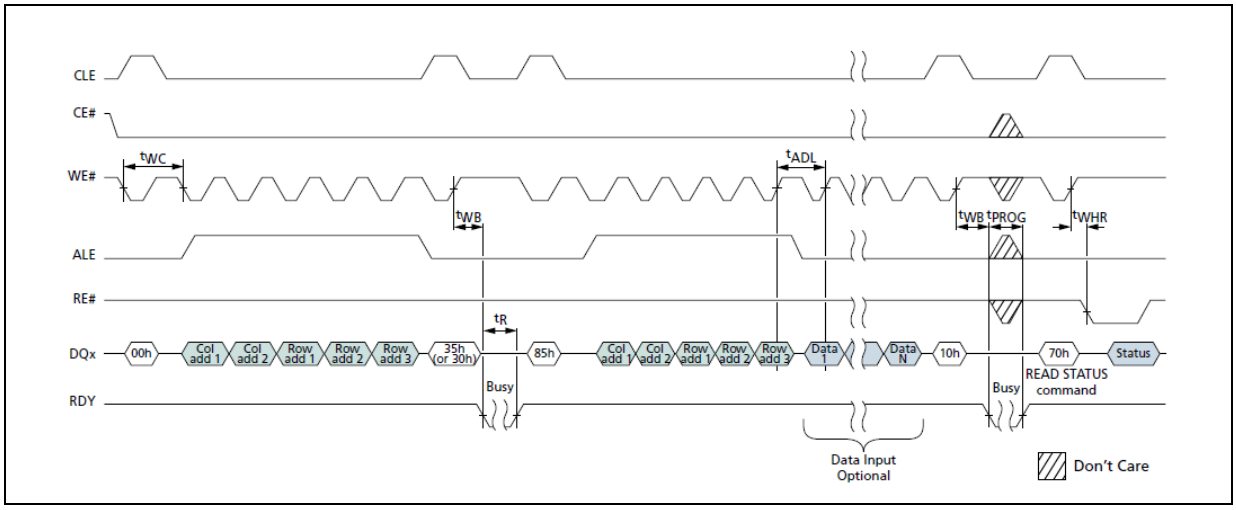
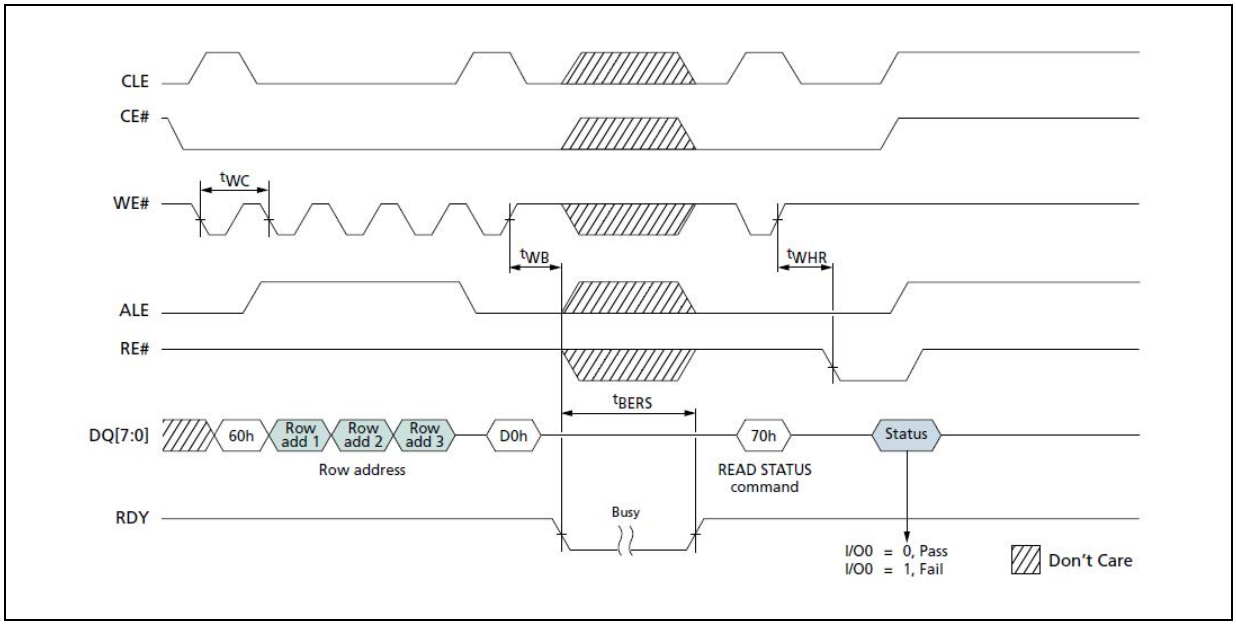
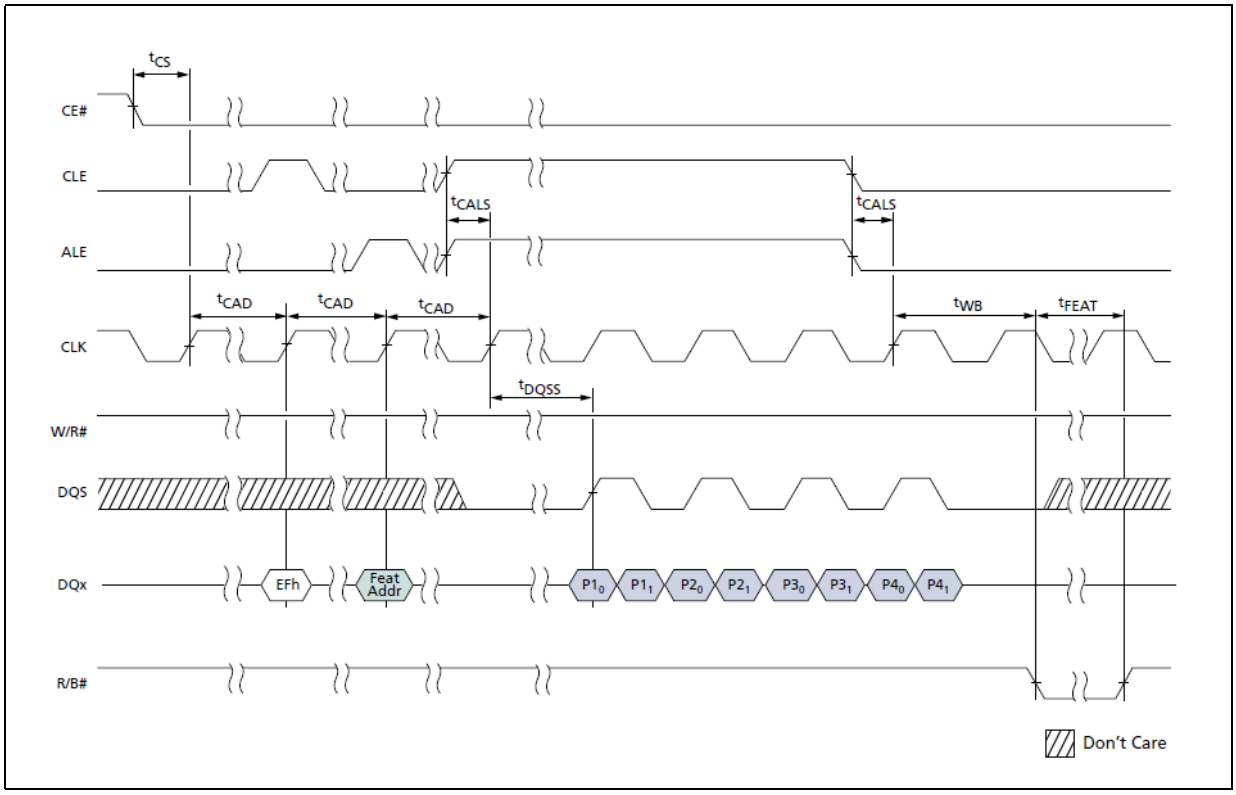


Figure 100. ERASE BLOCK Operation



35.0 Onfi 2.3 Interface Timing Diagrams

Figure 101. SET FEATURES Operation



Notes:

1. When CE# remains LOW, tCAD begins at the rising edge of the clock from which the last data byte is input for the subsequent command or data input cycle(s).
2. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
3. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).
4. The cycle that tCAD is measured from may be an idle cycle (as shown), another command cycle, an address cycle, or a data cycle. The idle cycle is shown in this diagram for simplicity.

Figure 102. READ ID Operation

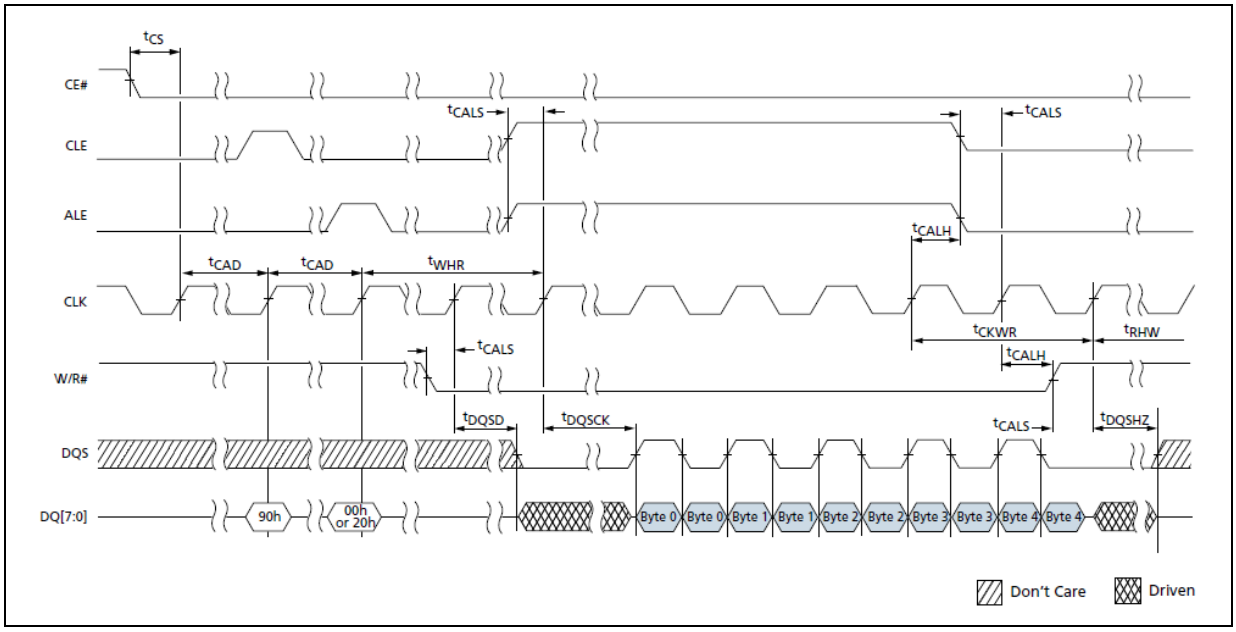


Figure 103. GET FEATURES Operation

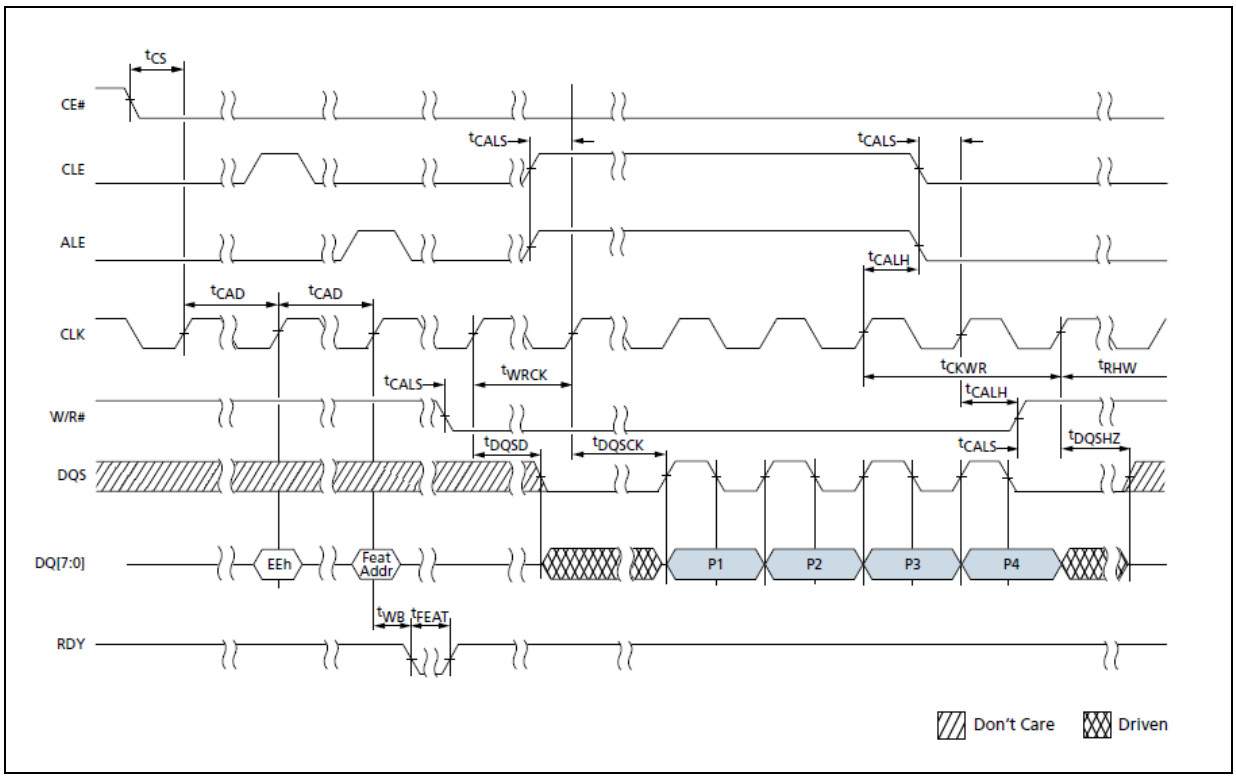


Figure 104. RESET (FCh) Operation

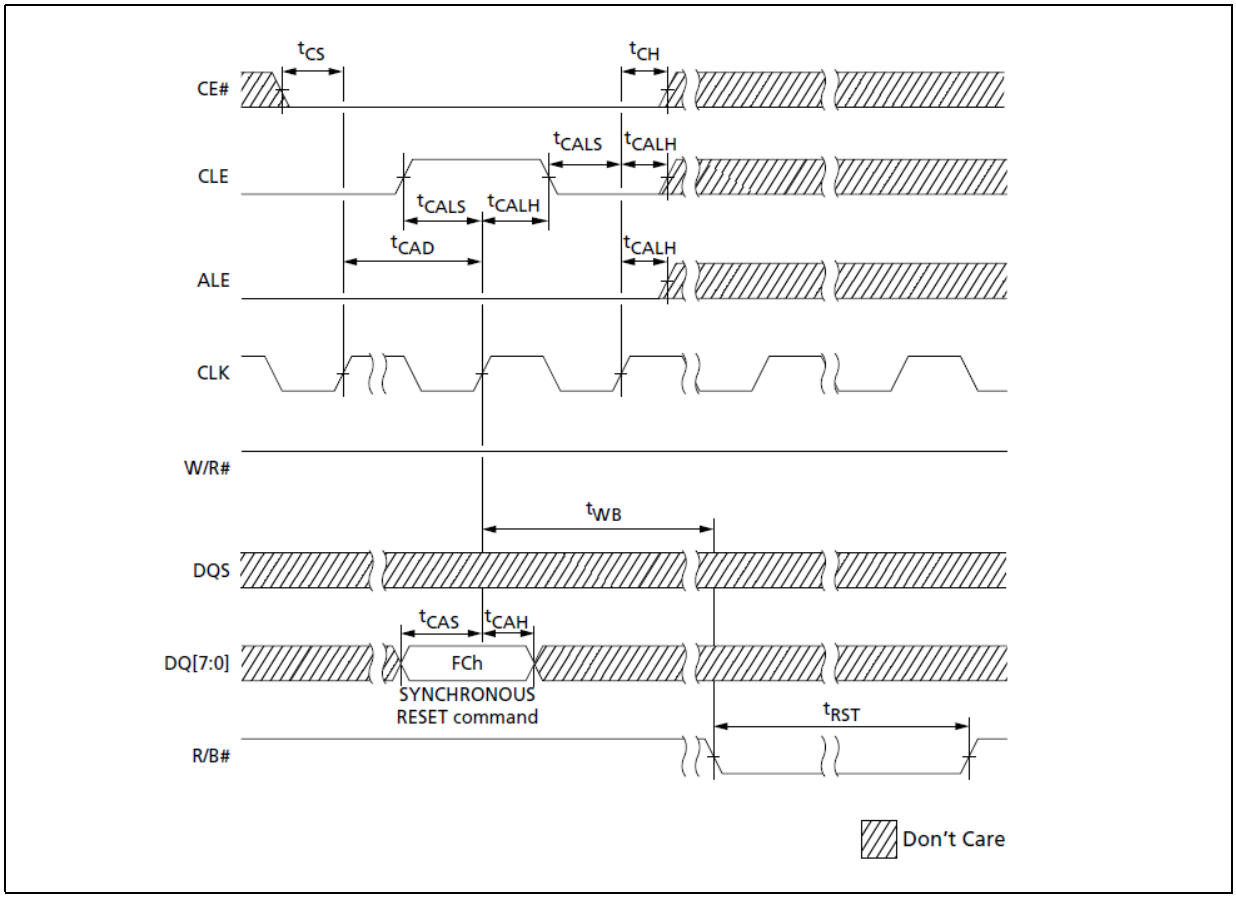


Figure 105. READ STATUS Cycle

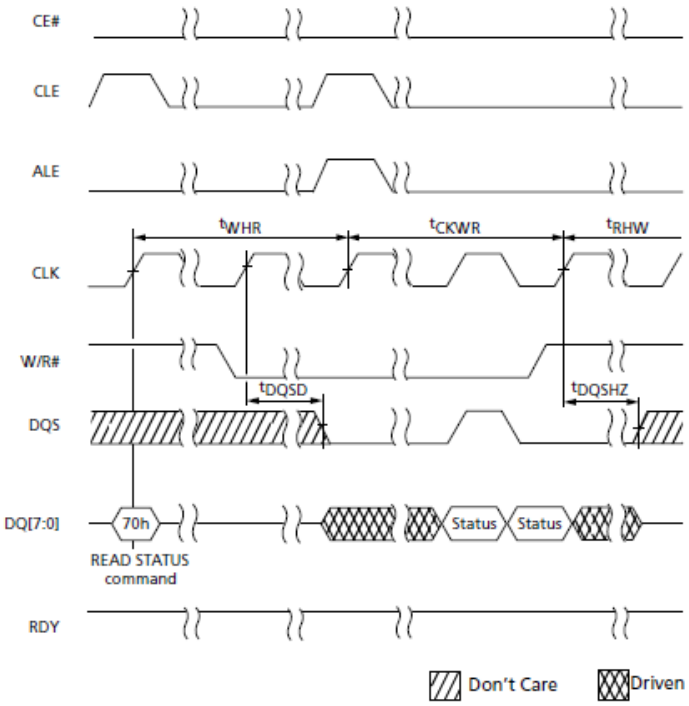


Figure 106. READ STATUS ENHANCED Operation

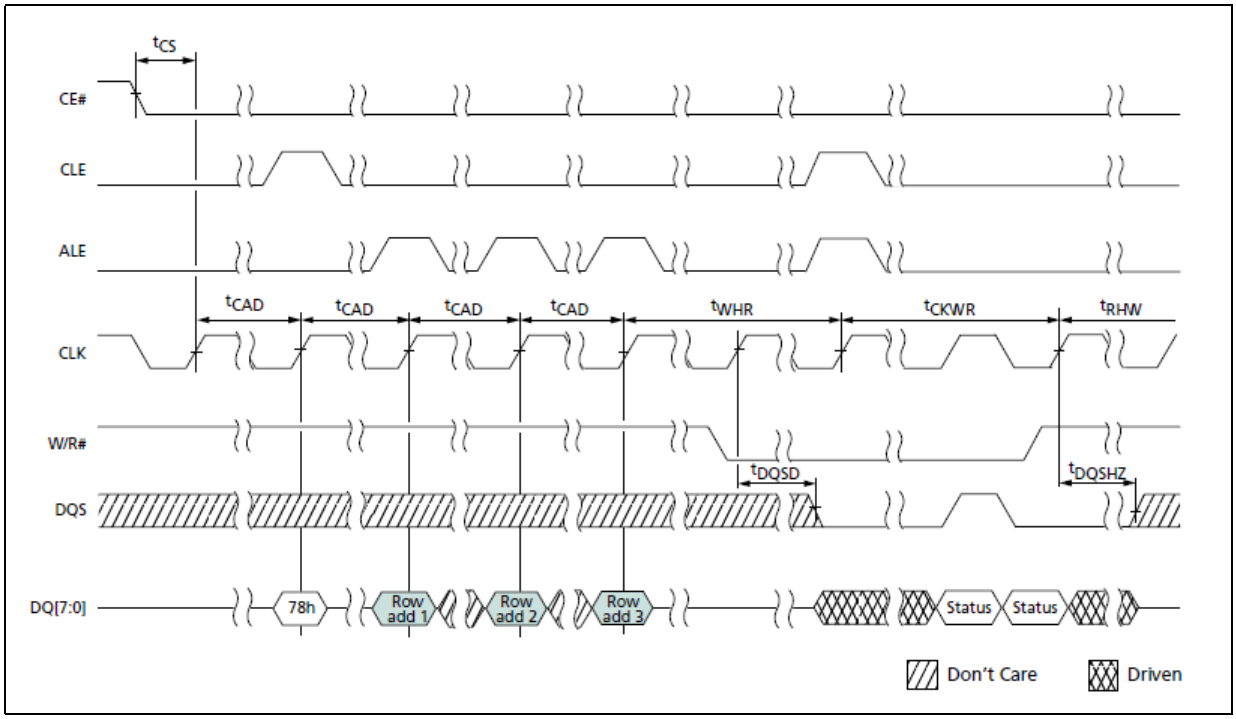


Figure 107. READ PARAMETER PAGE Operation

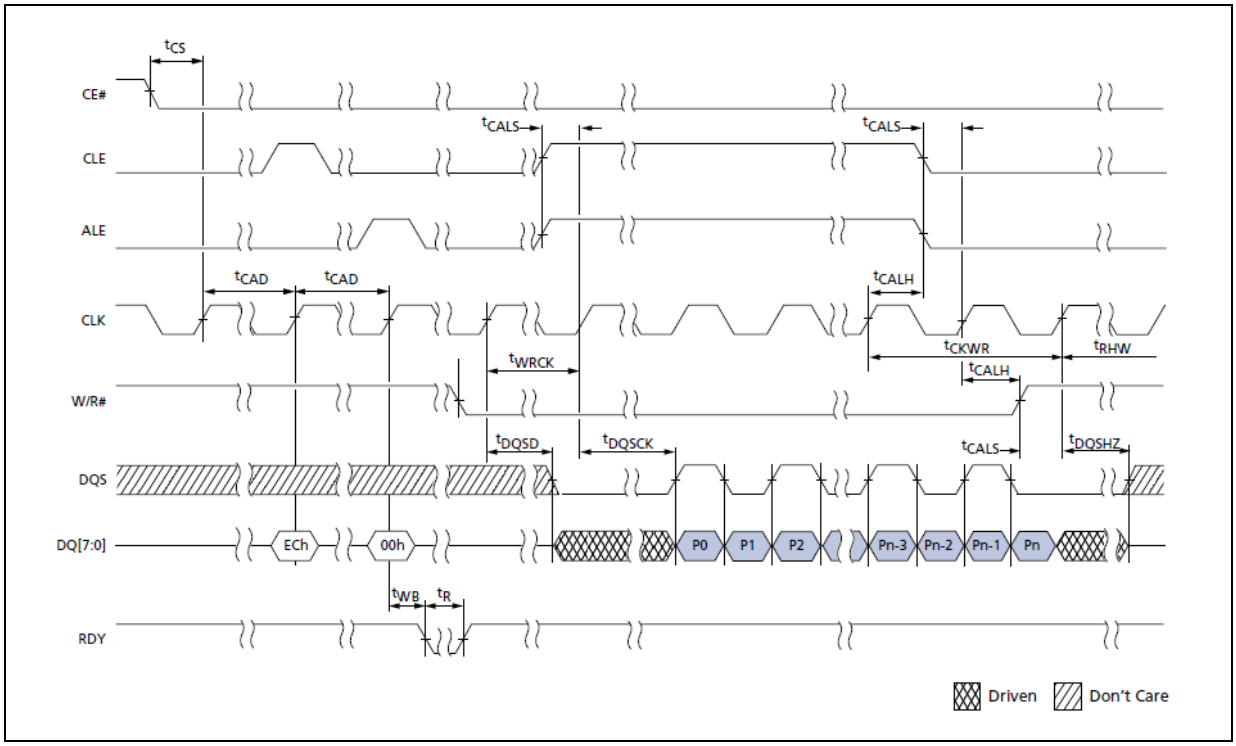


Figure 108. READ PAGE Operation

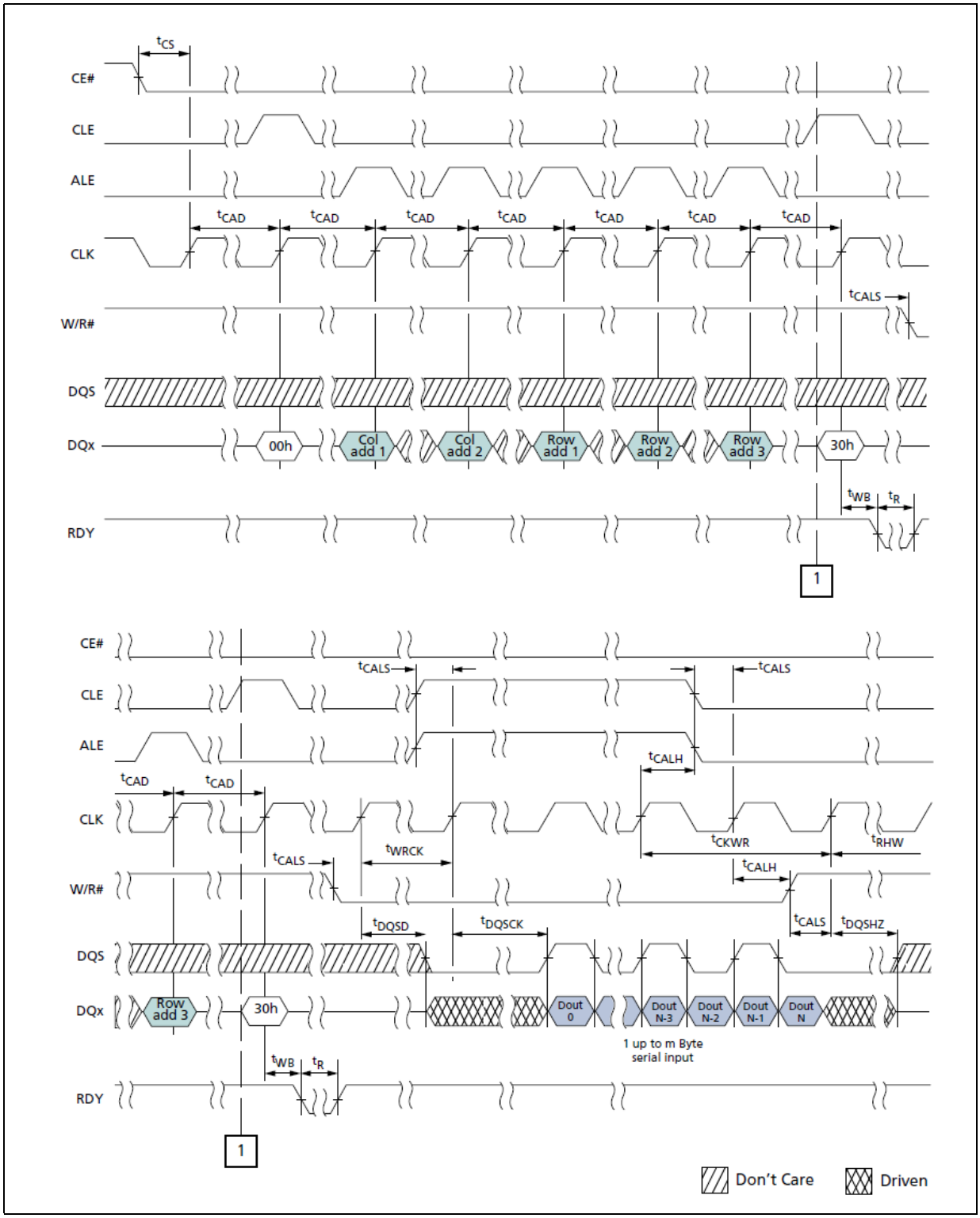


Figure 109. CHANGE READ Column

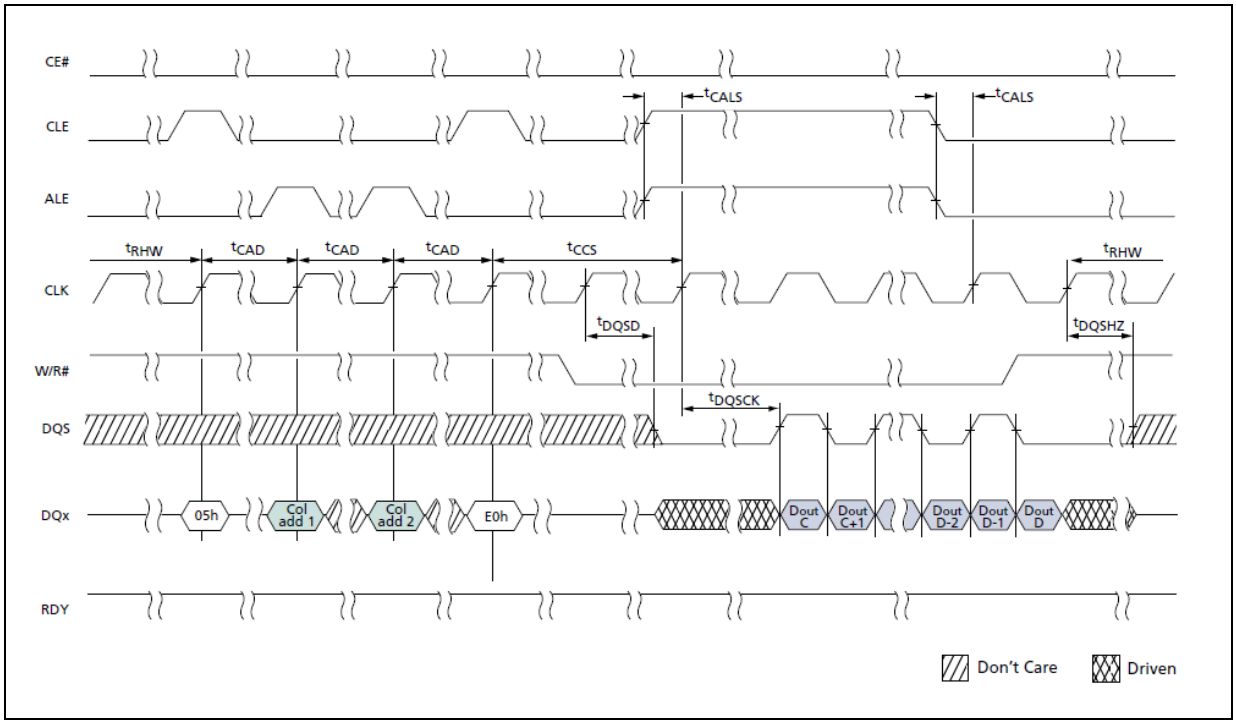


Figure 110. READ PAGE CACHE SEQUENTIAL (1 of 2)

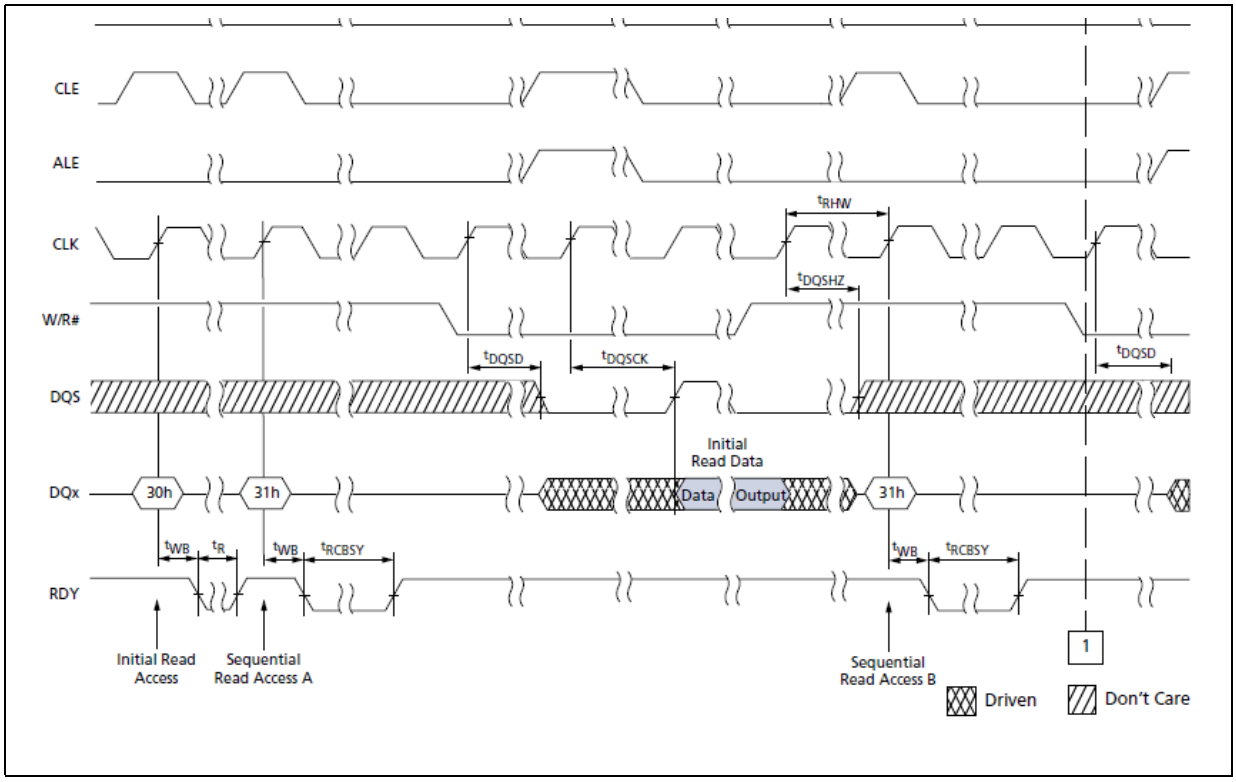


Figure 111. READ PAGE CACHE SEQUENTIAL (2 of 2)

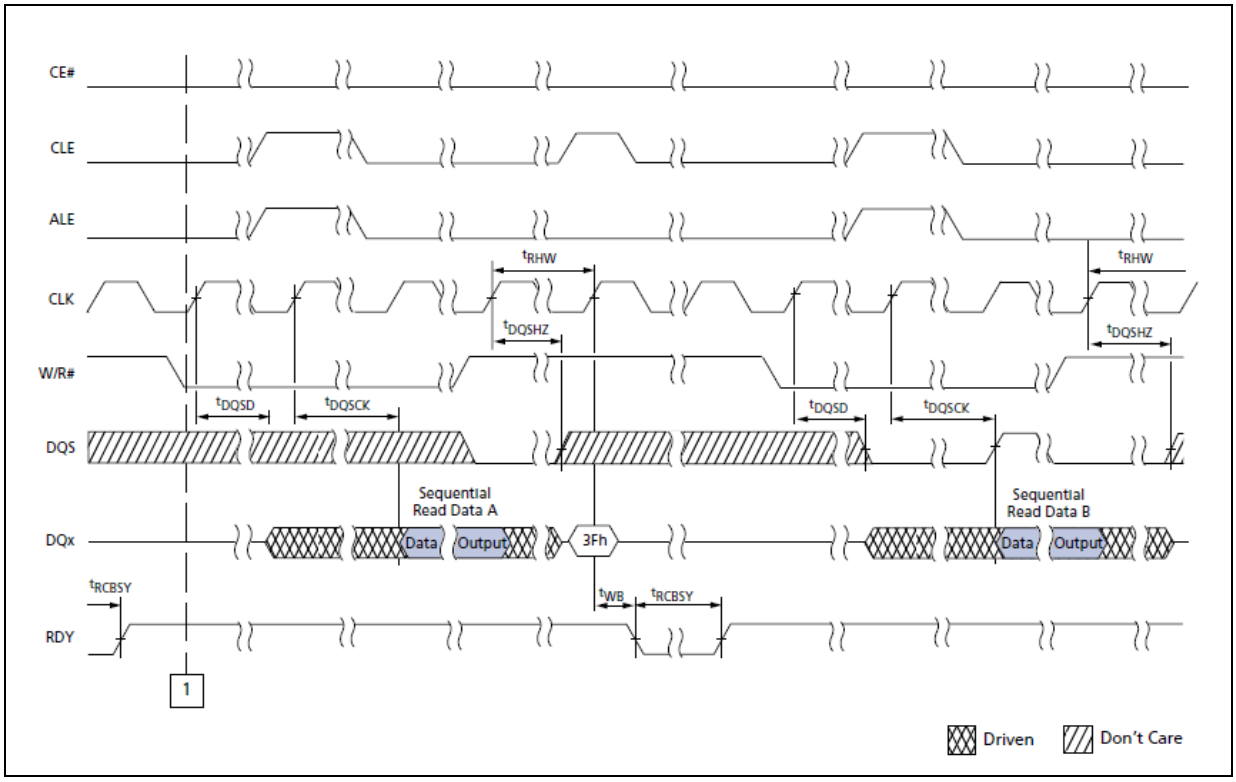


Figure 112. READ PAGE CACHE RANDOM (1 of 2)

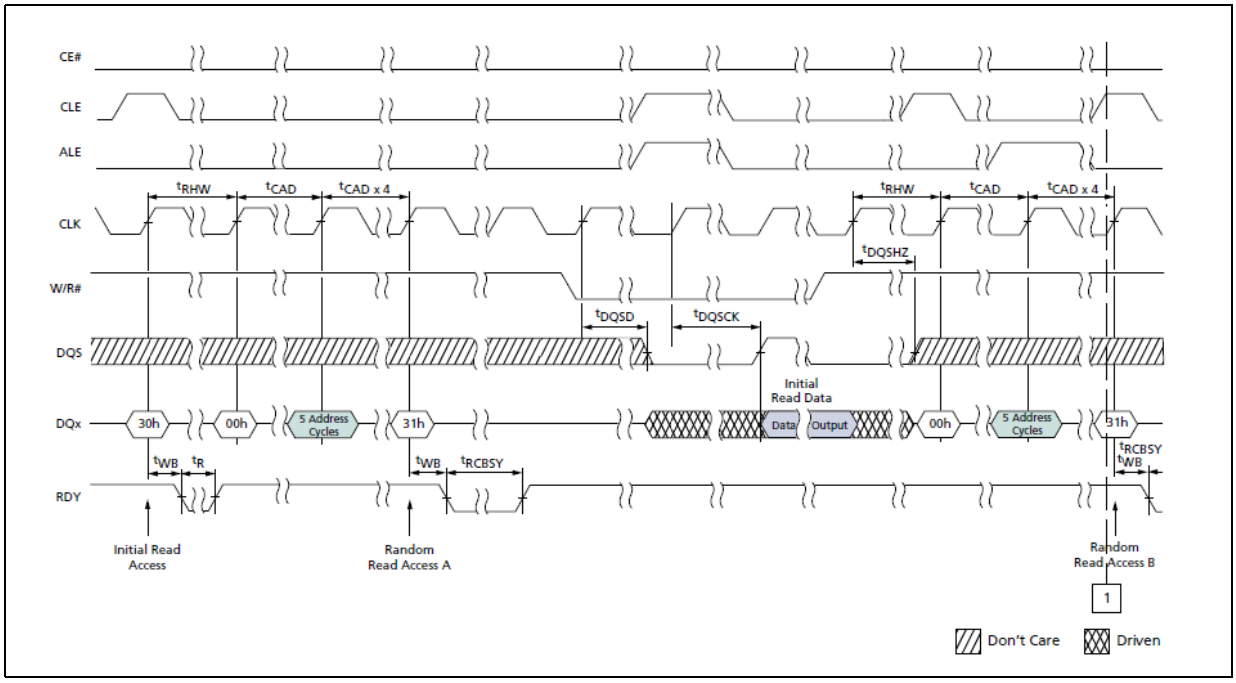


Figure 113. READ PAGE CACHE RANDOM (2 of 2)

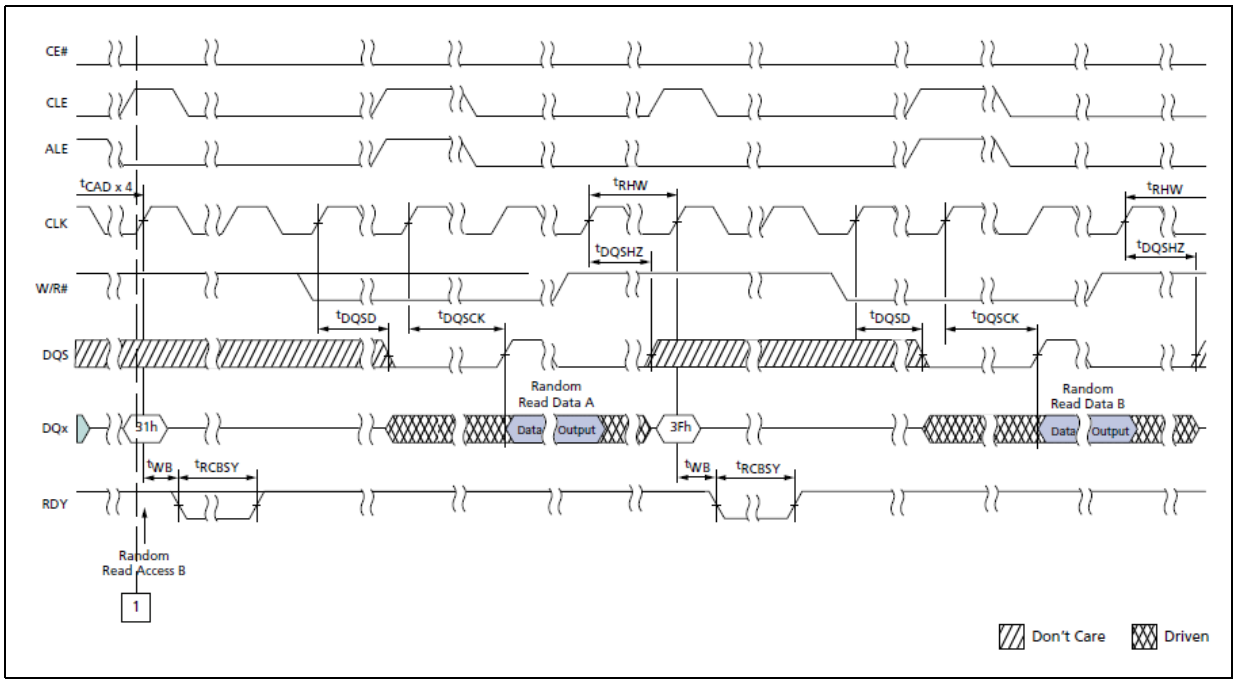


Figure 114. Multi-Plane Read Page (1 of 2)

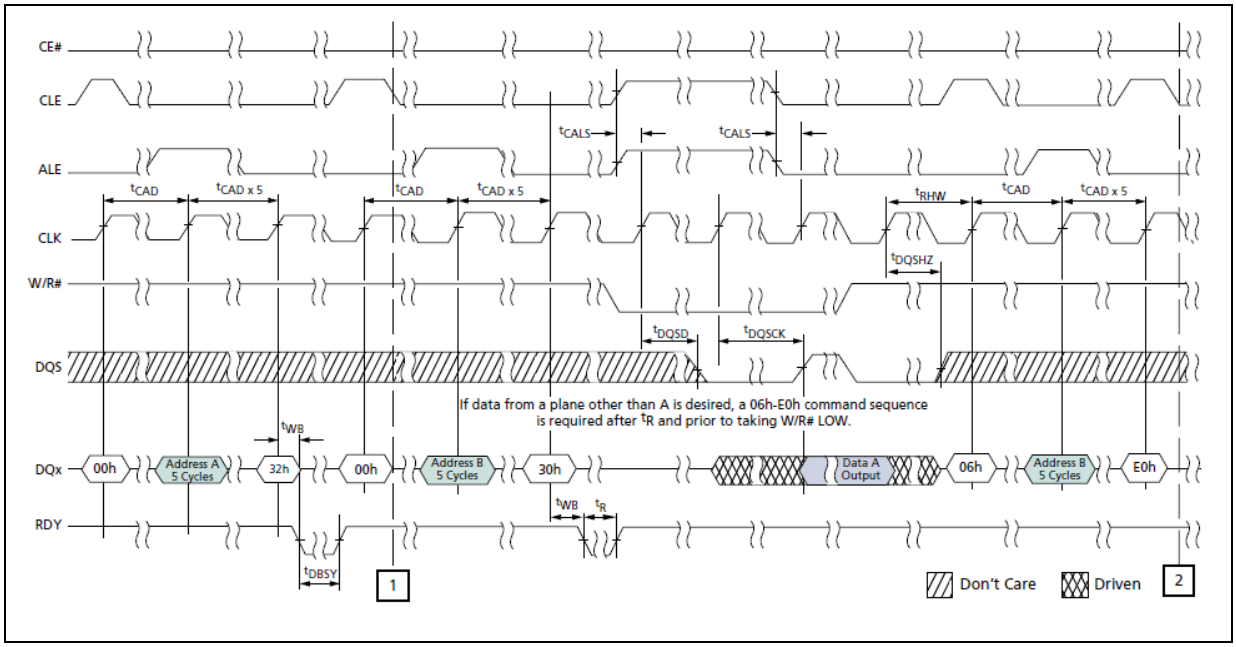


Figure 115. Multi-Plane Read Page (2 of 2)

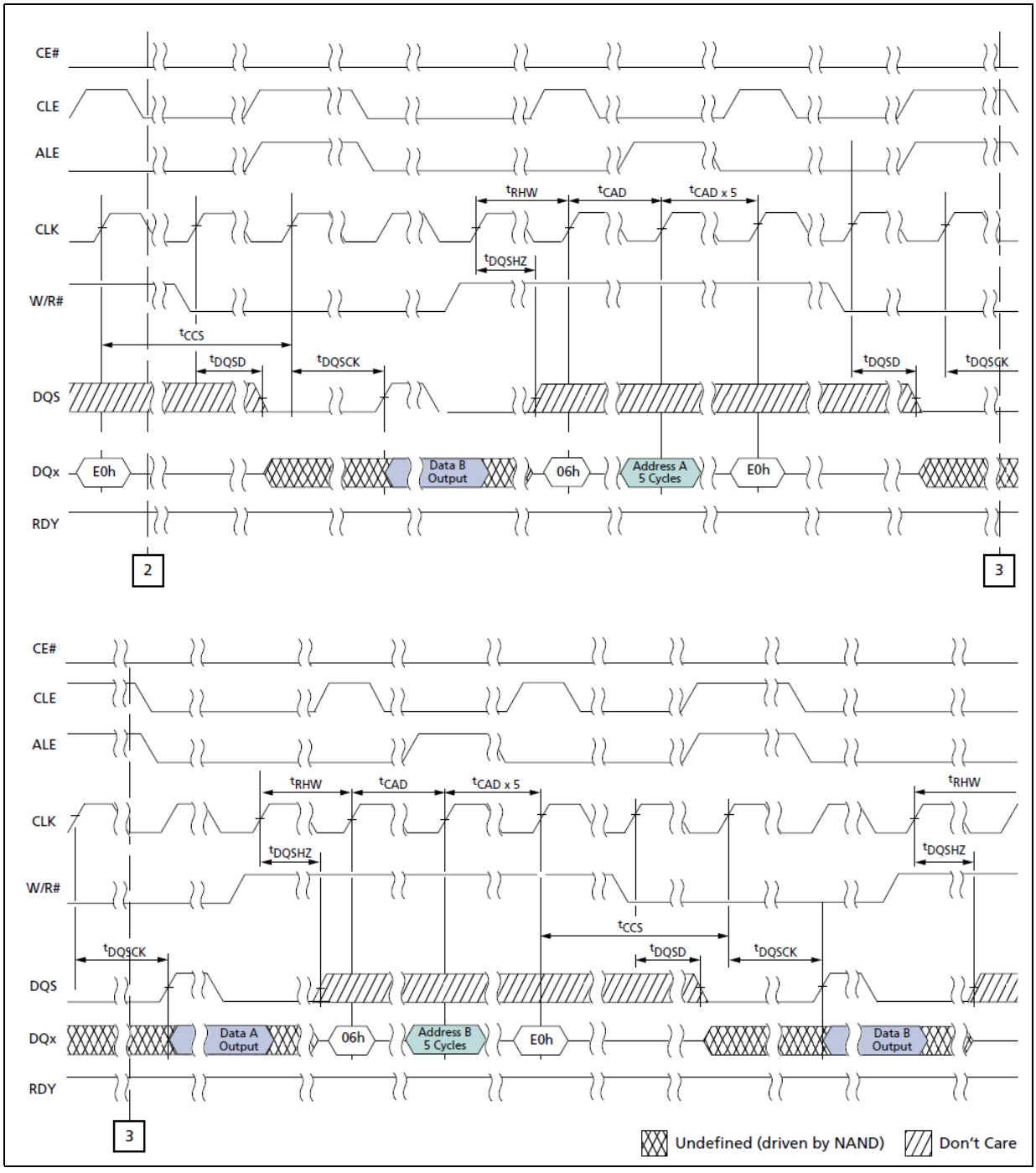


Figure 116. Program Page Operation (1 of 2)

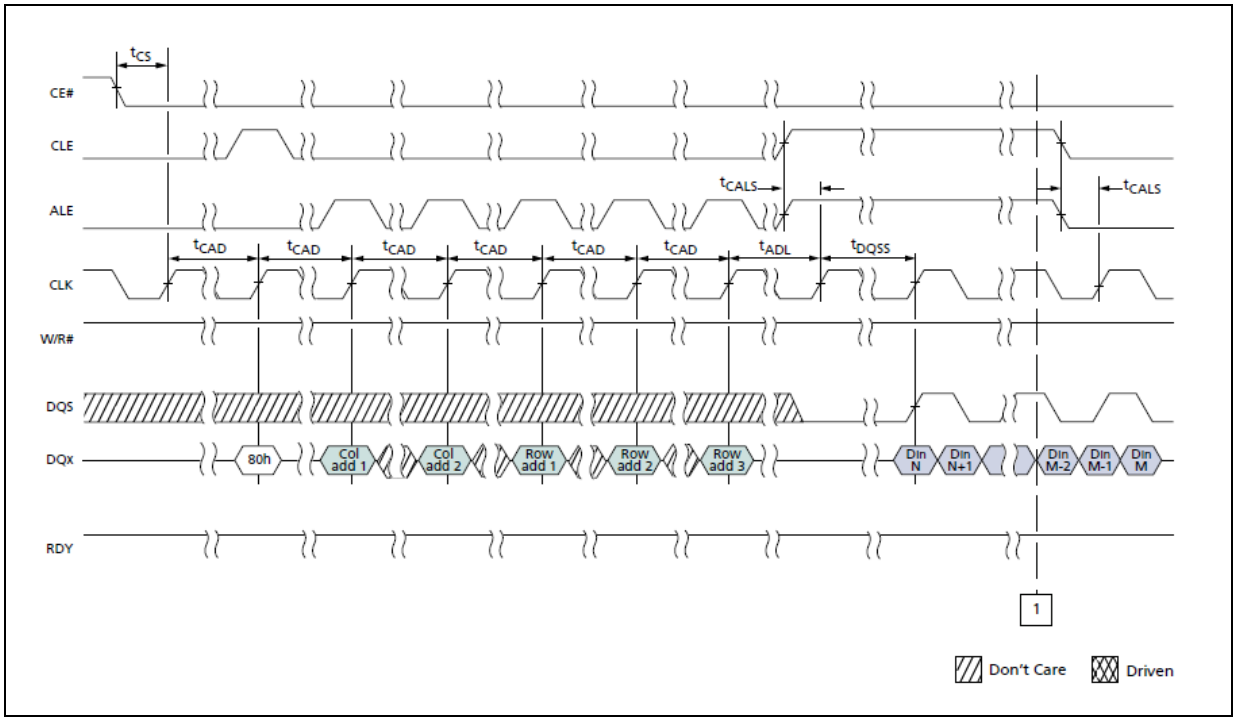


Figure 117. Program Page Operation (2 of 2)

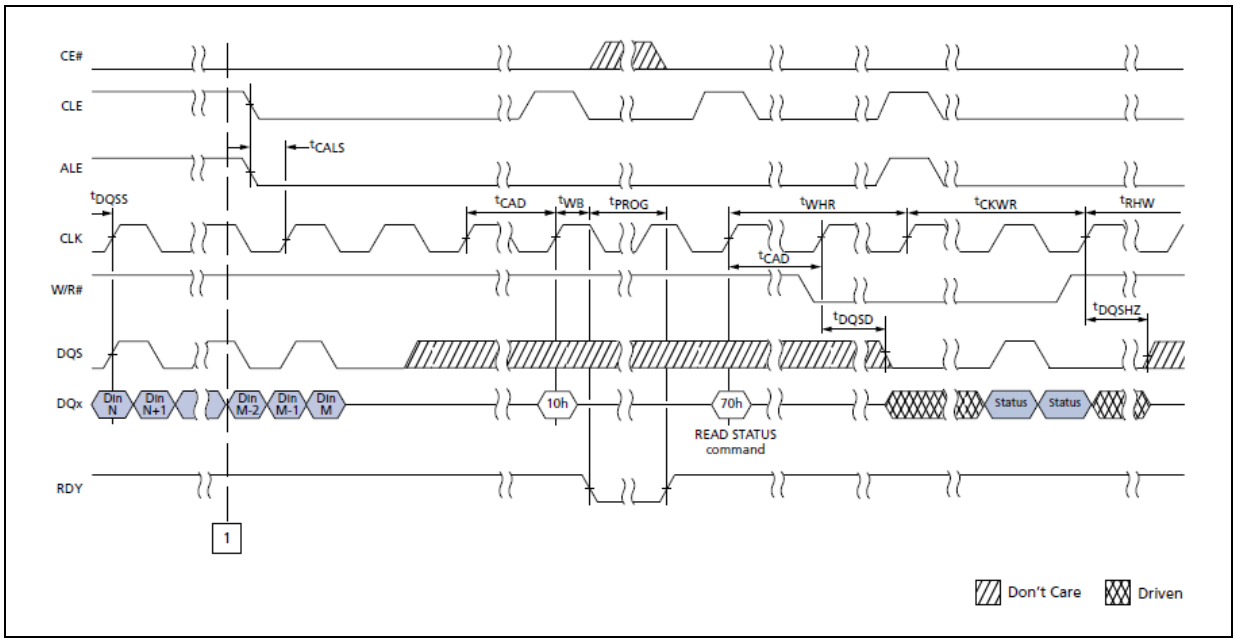


Figure 118. CHANGE WRITE COLUMN

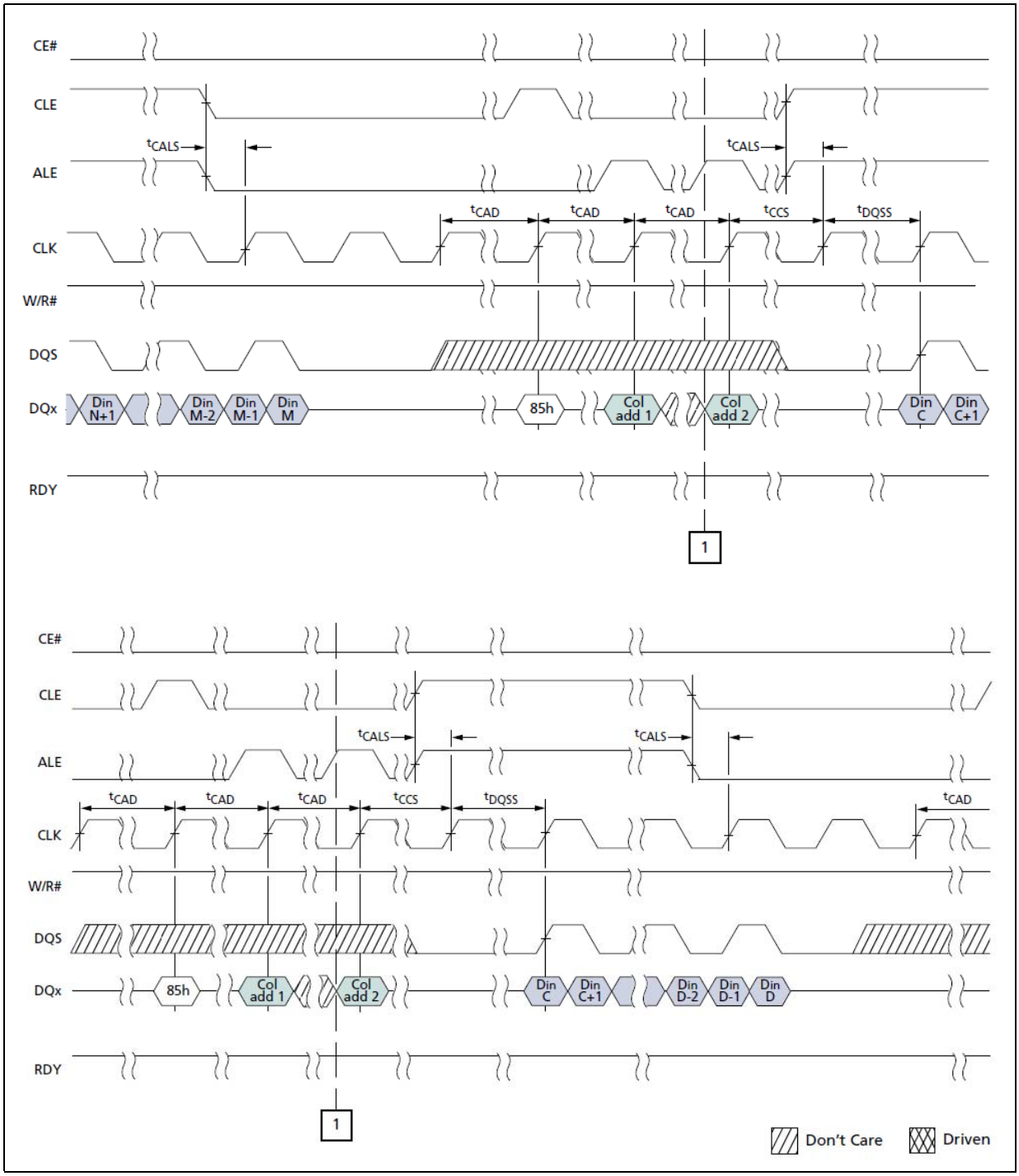


Figure 119. Multi-Plane Program Page

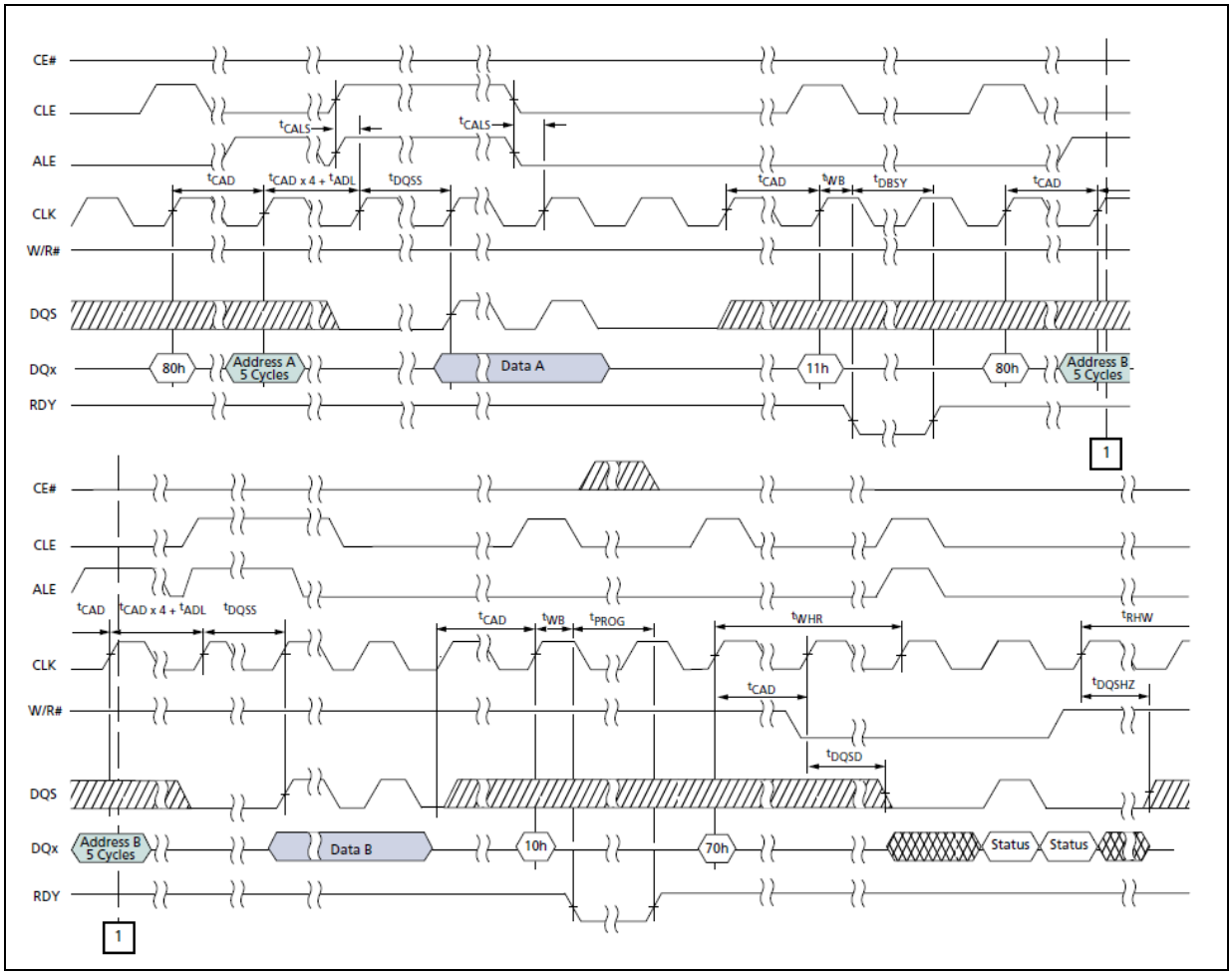


Figure 120. ERASE BLOCK

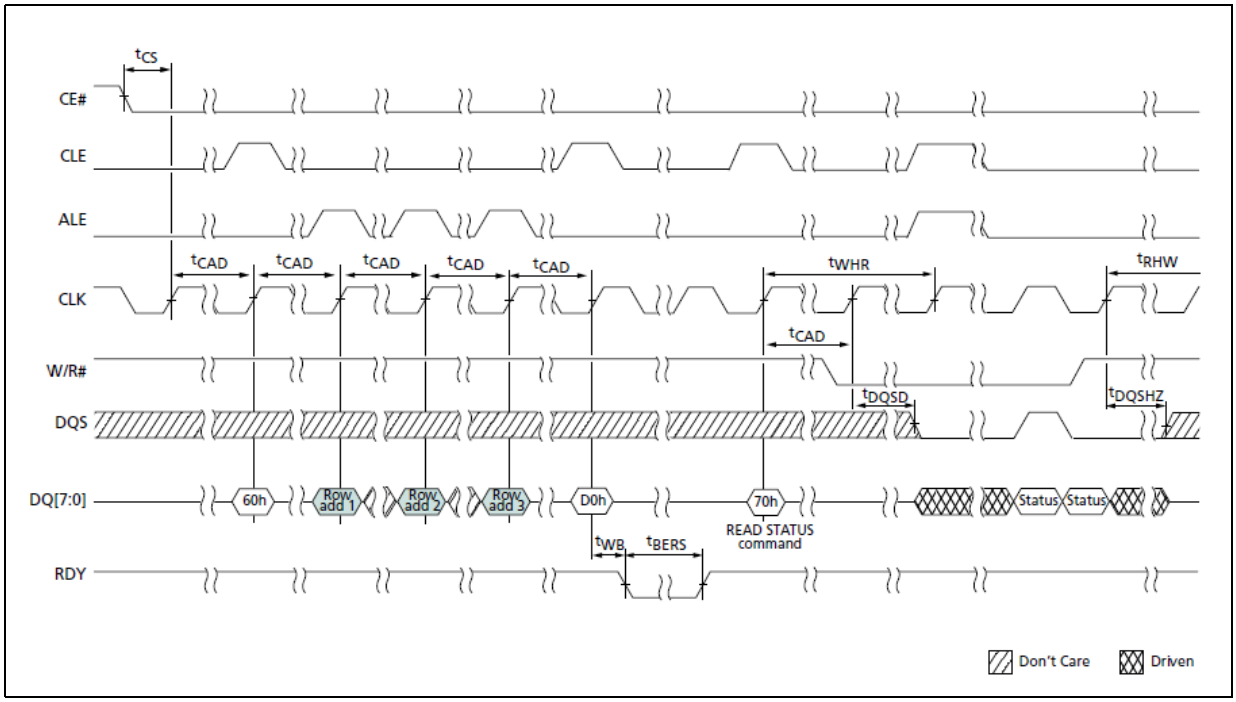


Figure 121. COPYBACK (1 of 3)

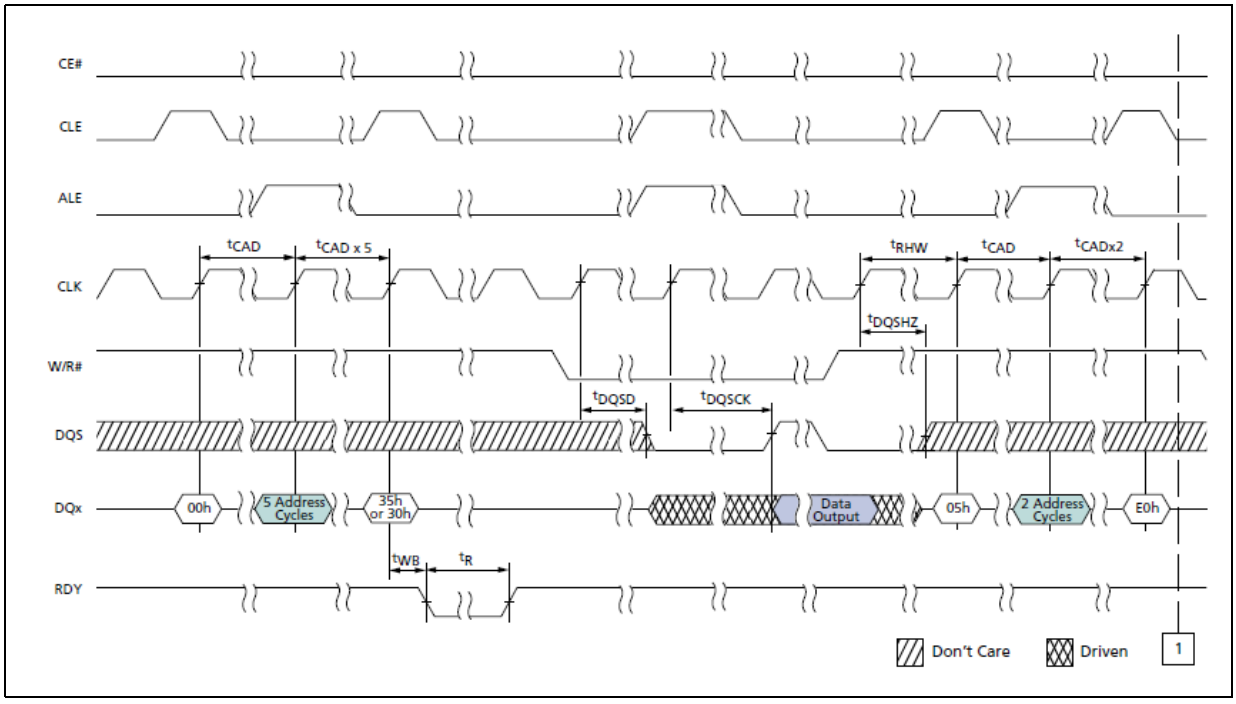


Figure 122. COPYBACK (2 of 3)

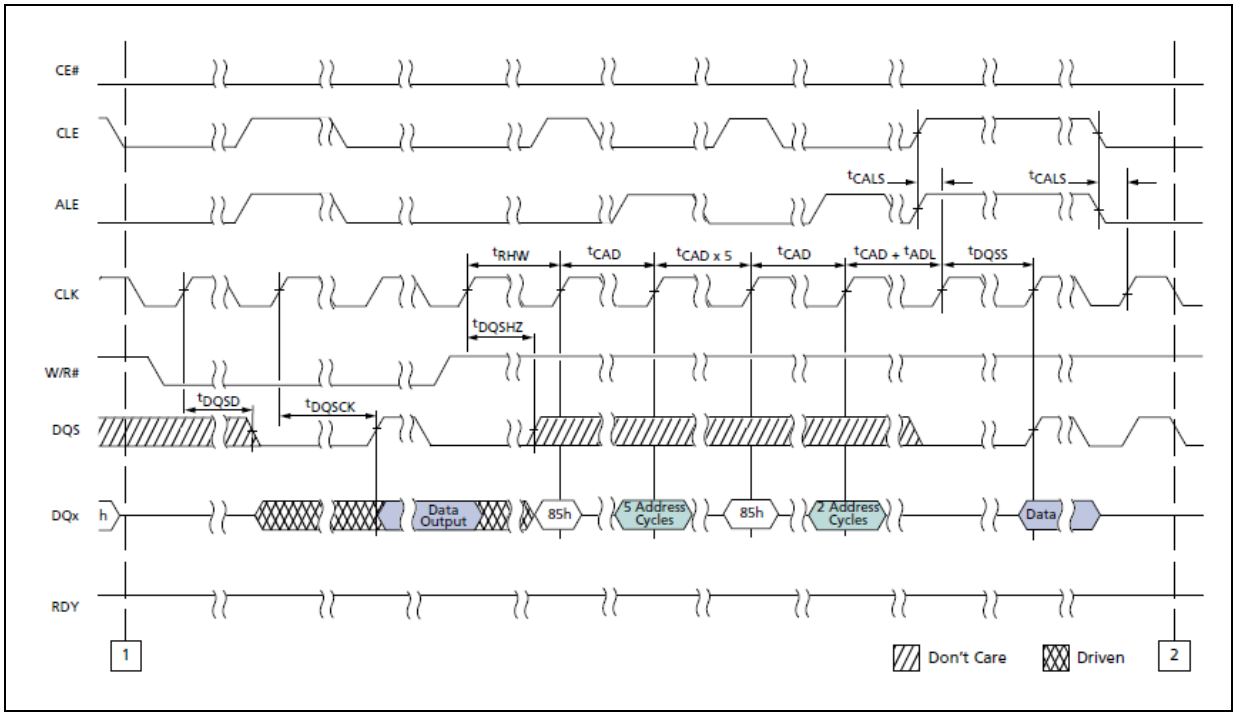
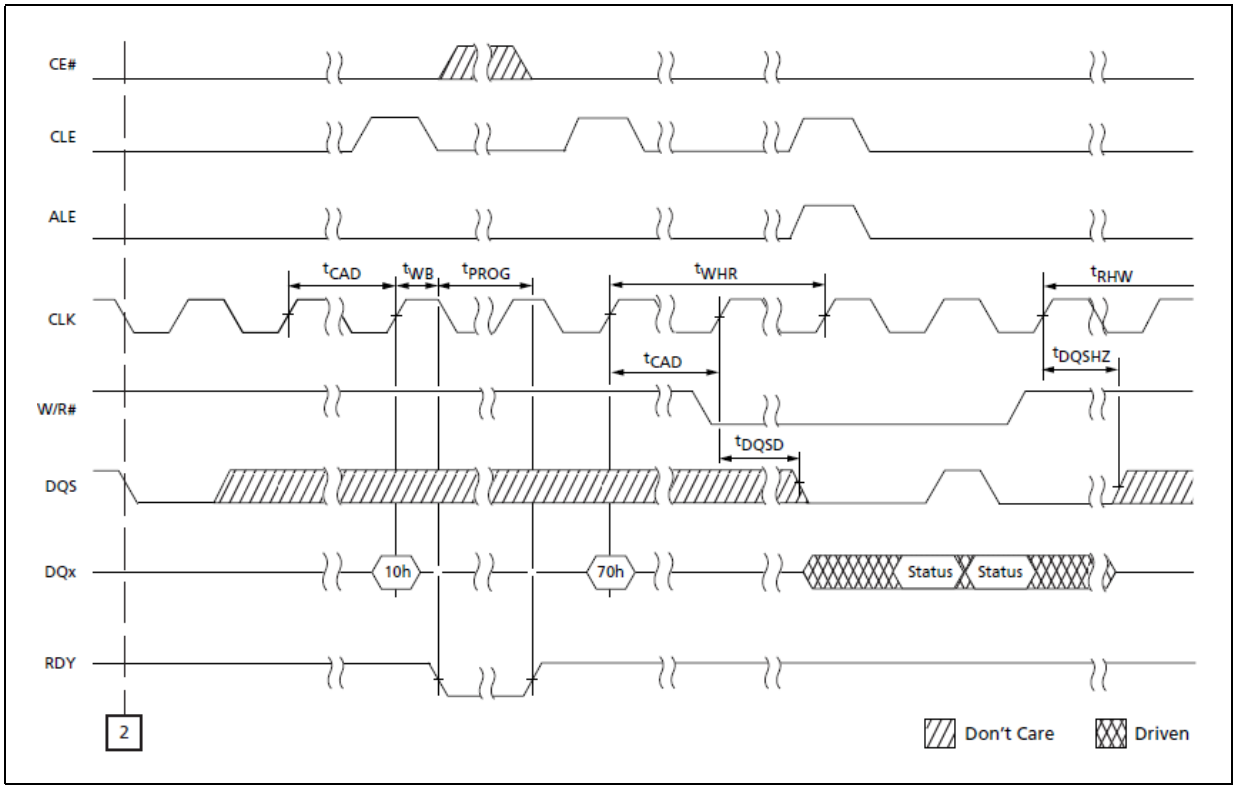


Figure 123. COPYBACK (3 of 3)



36.0 Onfi 3.0 Interface Timing Diagrams

Figure 124. SET FEATURES Operation

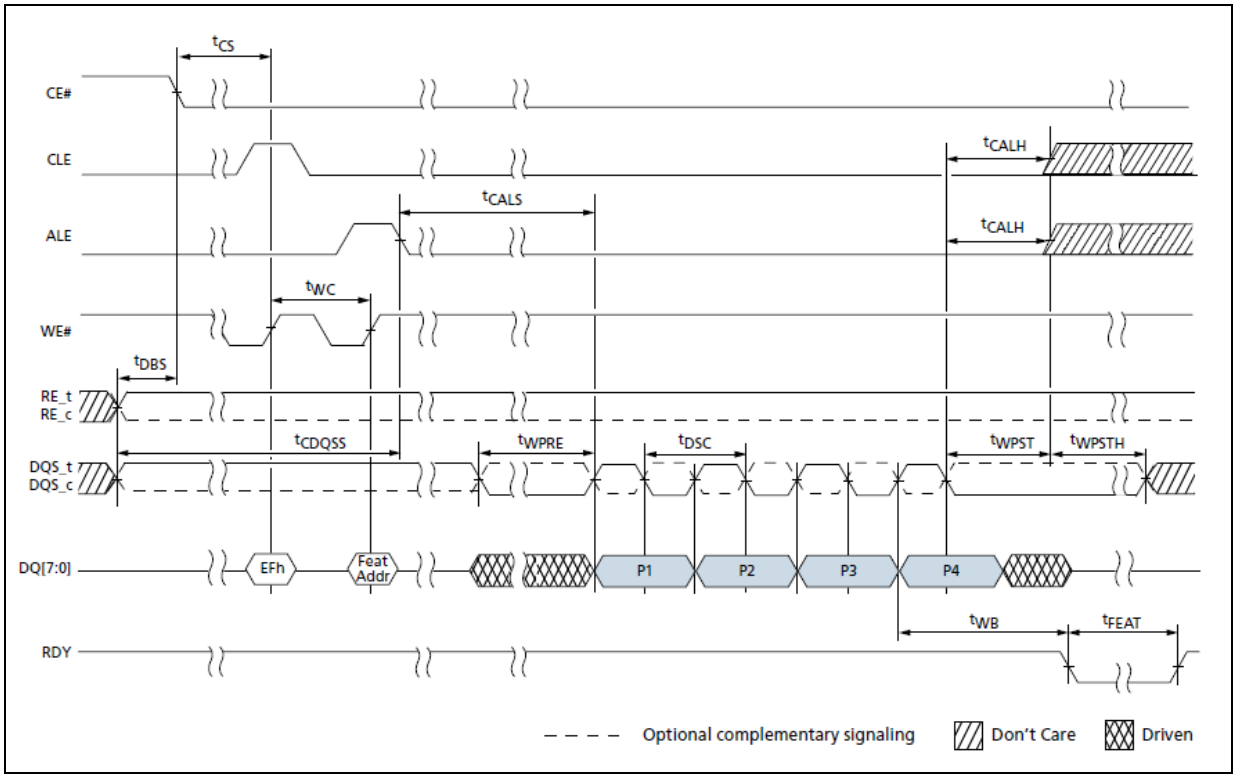


Figure 125. READ ID Operation

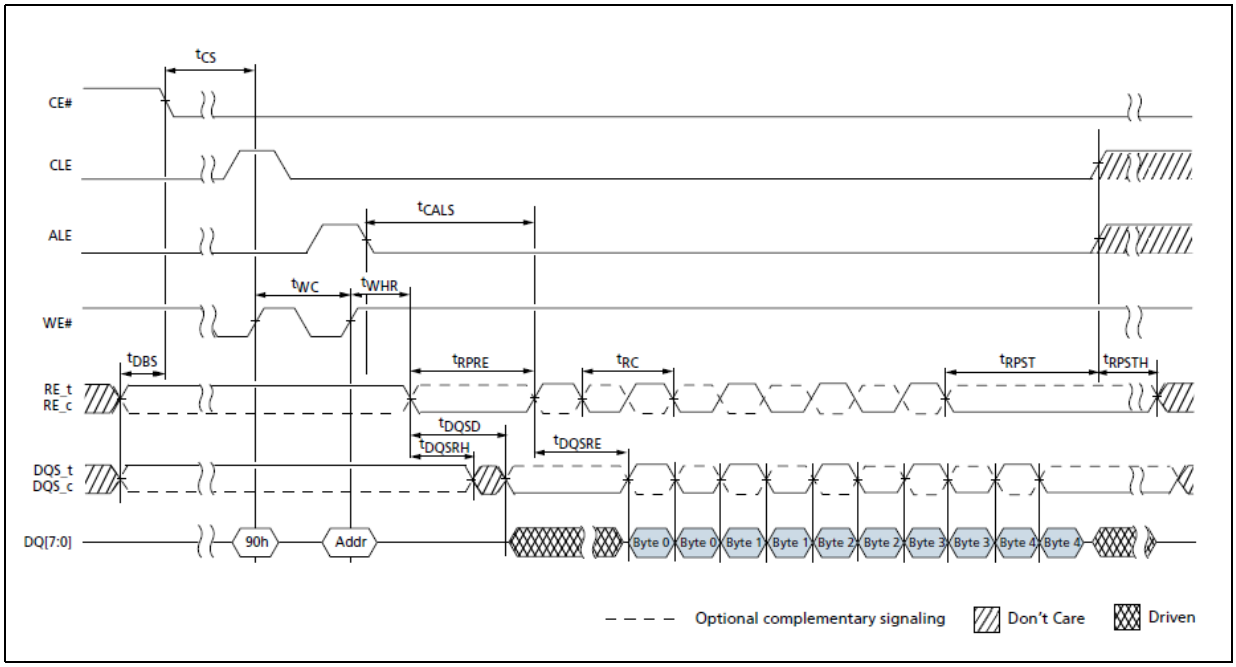


Figure 126. GET FEATURES Operation

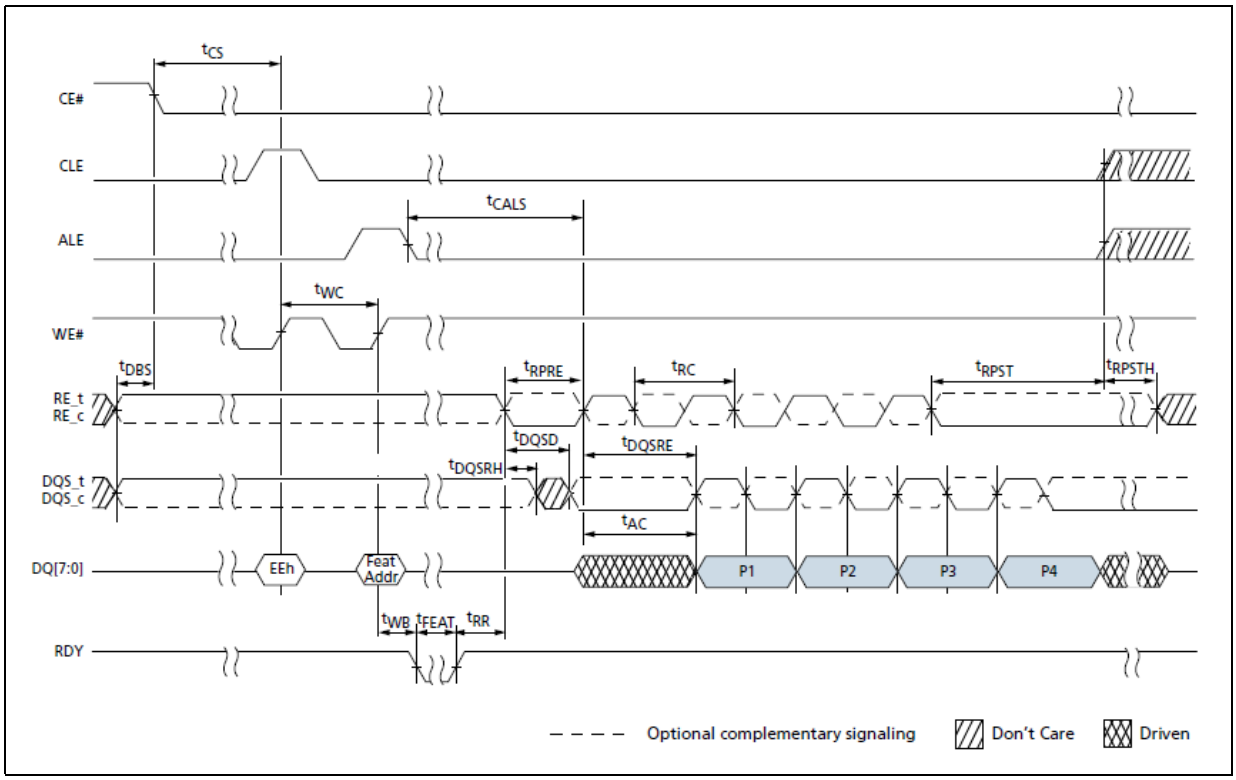


Figure 127. RESET (FCh) Operation

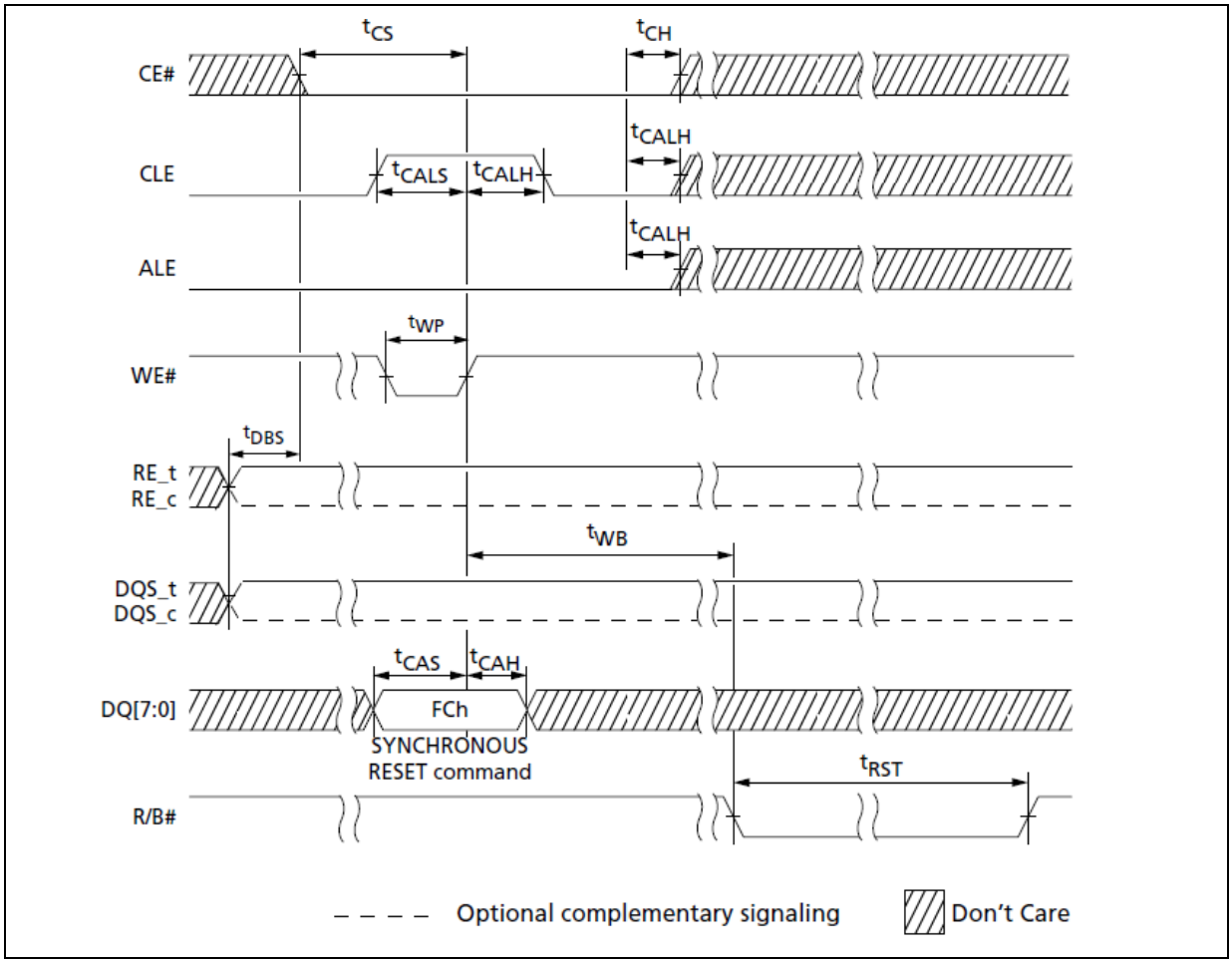


Figure 128. READ STATUS Cycle

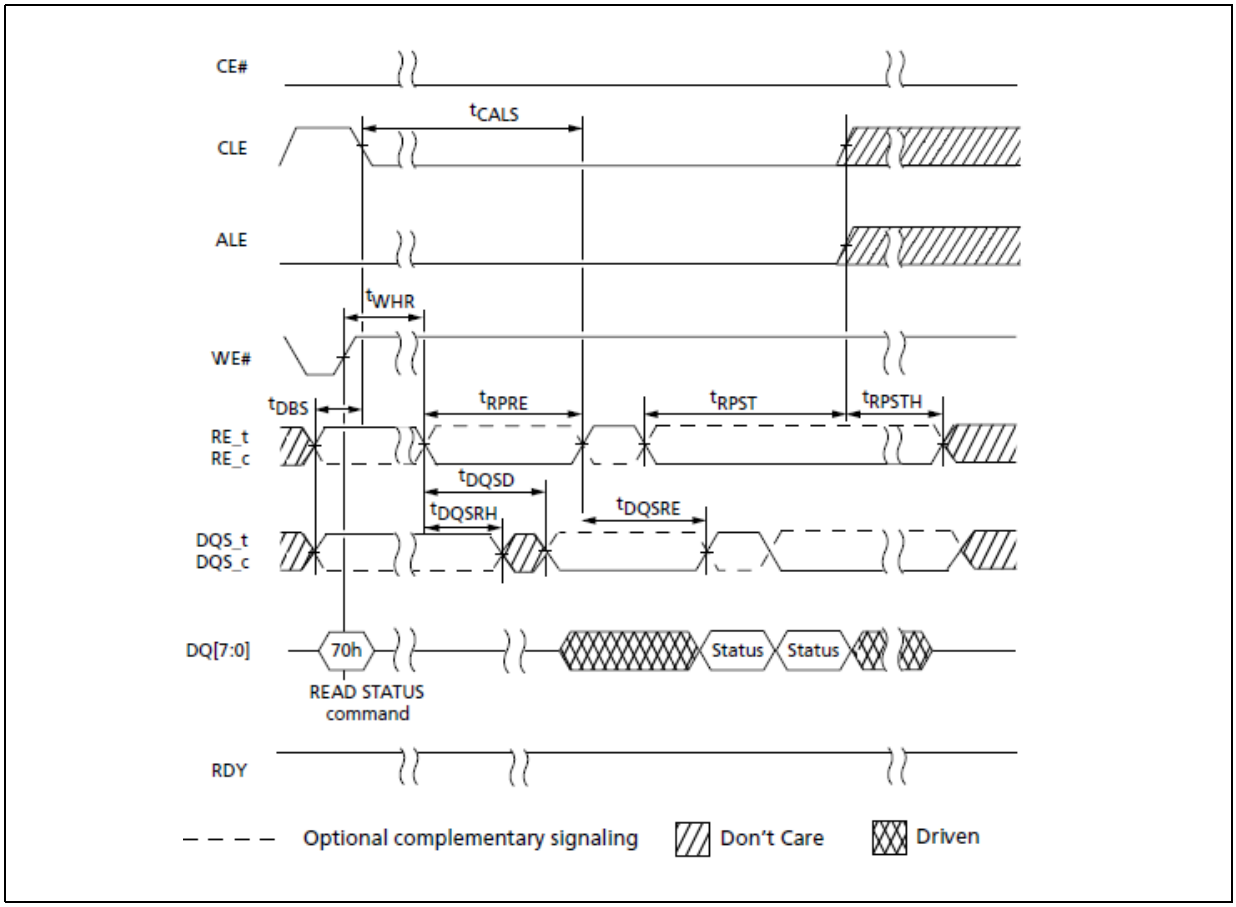


Figure 129. READ STATUS ENHANCED Operation

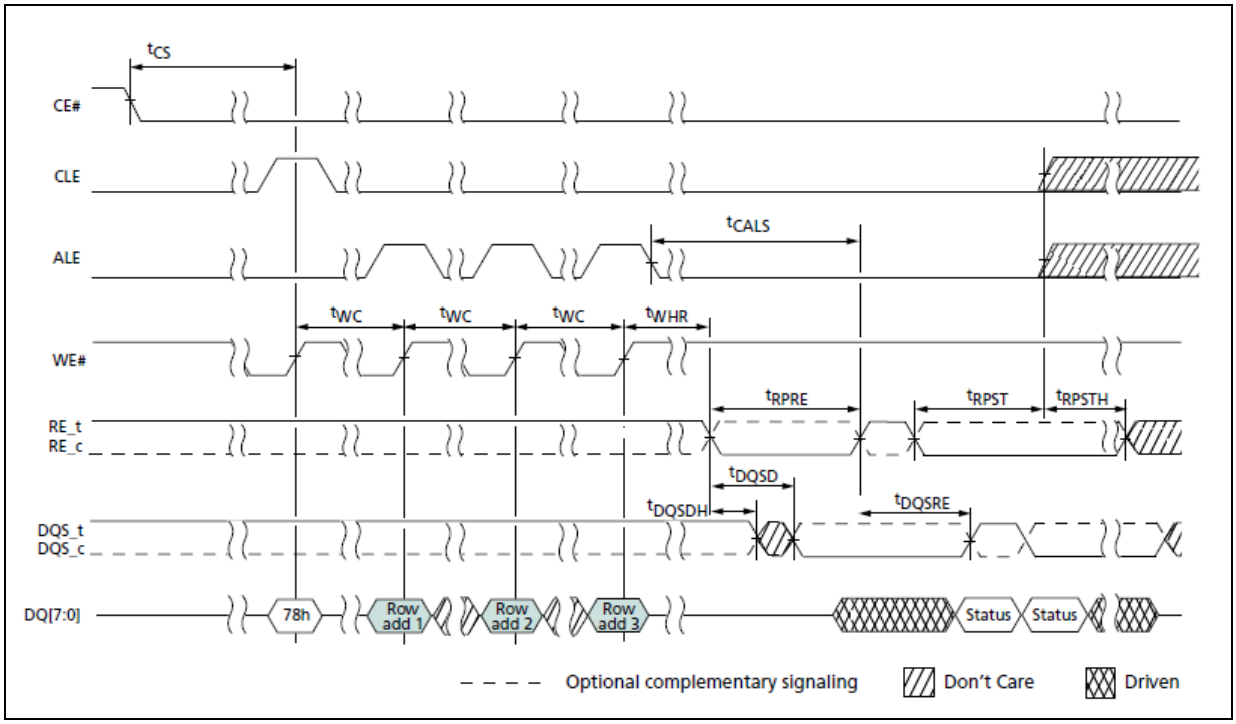


Figure 130. READ PARAMETER PAGE Operation

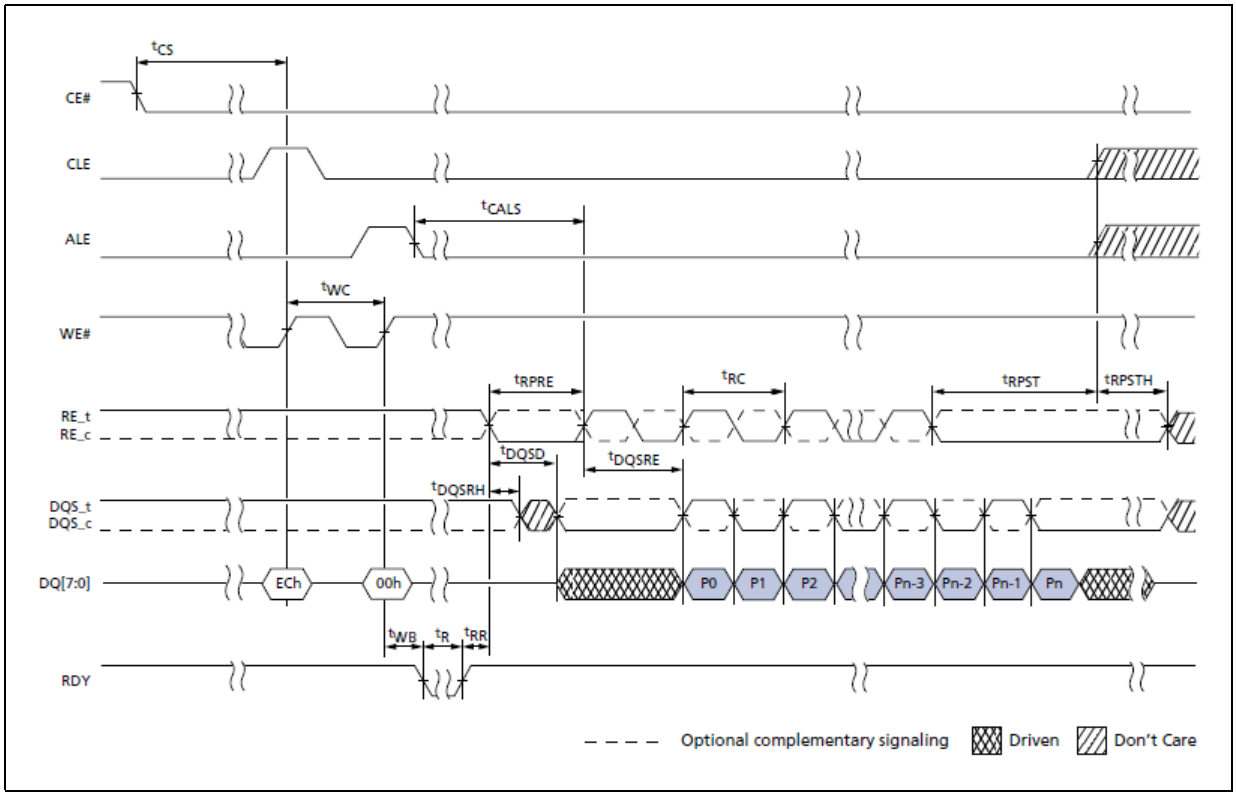


Figure 131. READ PAGE Operation

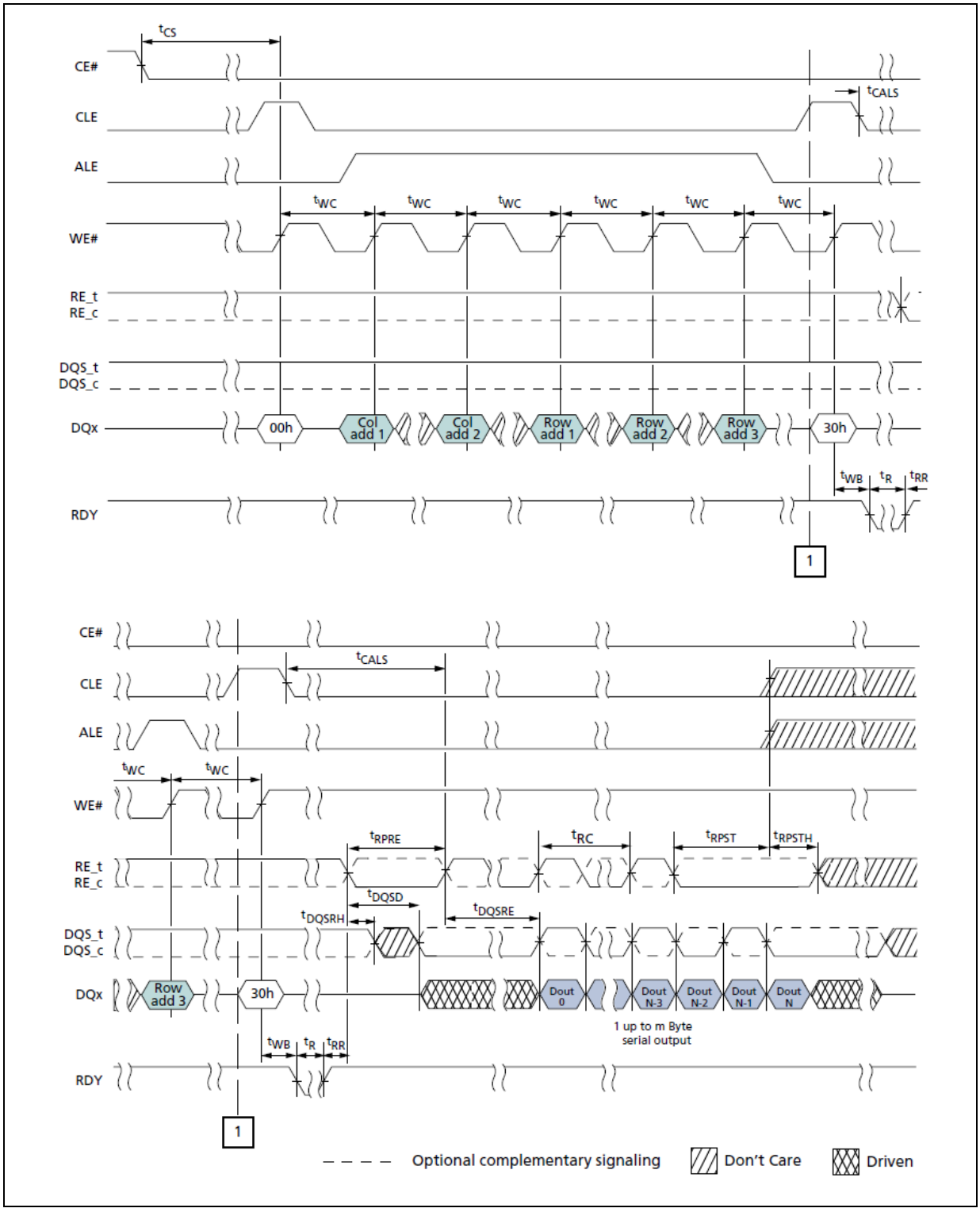


Figure 132. CHANGE READ COLUMN

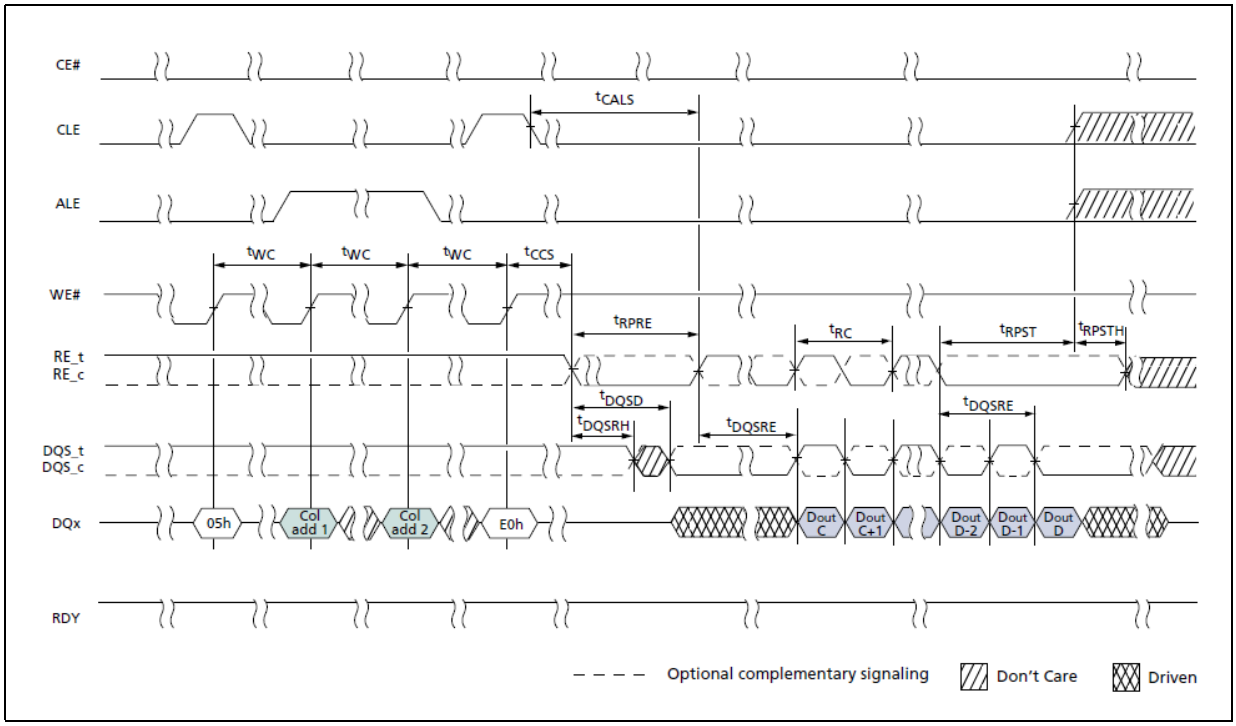


Figure 133. READ PAGE CACHE SEQUENTIAL (1 of 2)

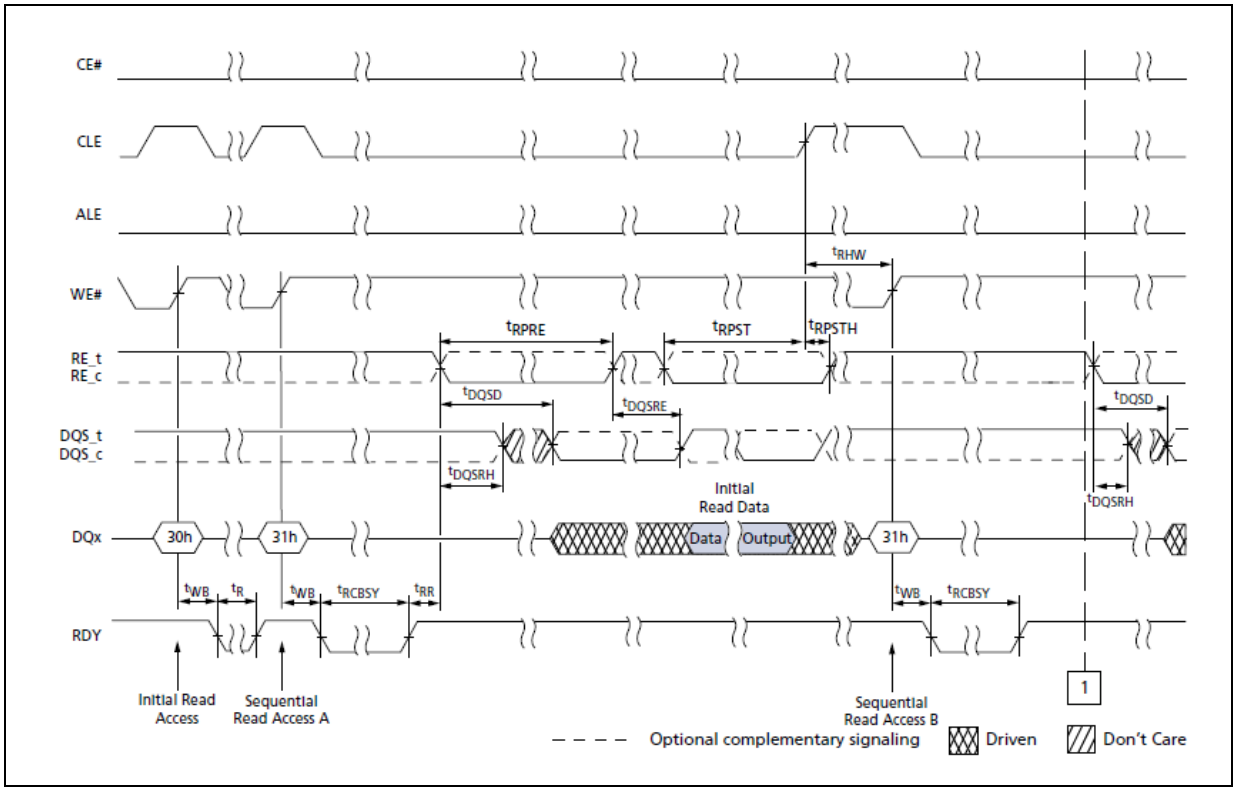


Figure 134. READ PAGE CACHE SEQUENTIAL (2 of 2)

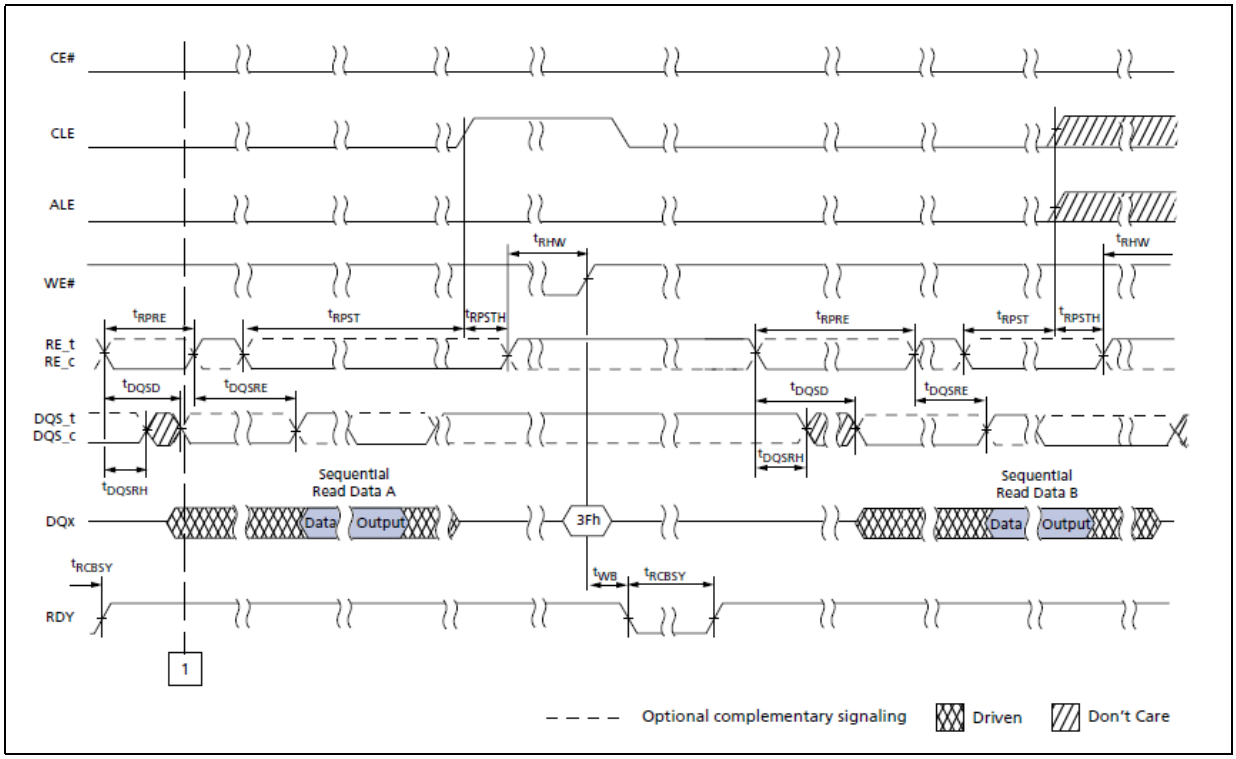


Figure 135. READ PAGE CACHE RANDOM (1 of 2)

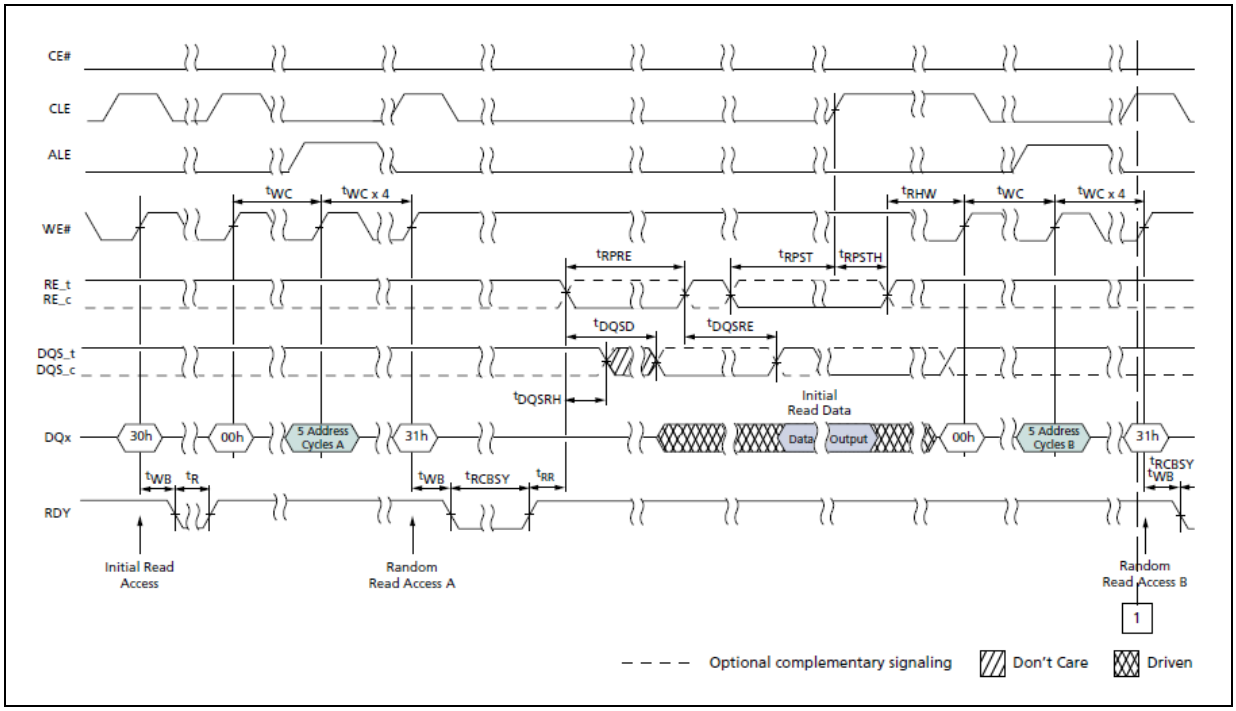


Figure 136. READ PAGE CACHE RANDOM (2 of 2)

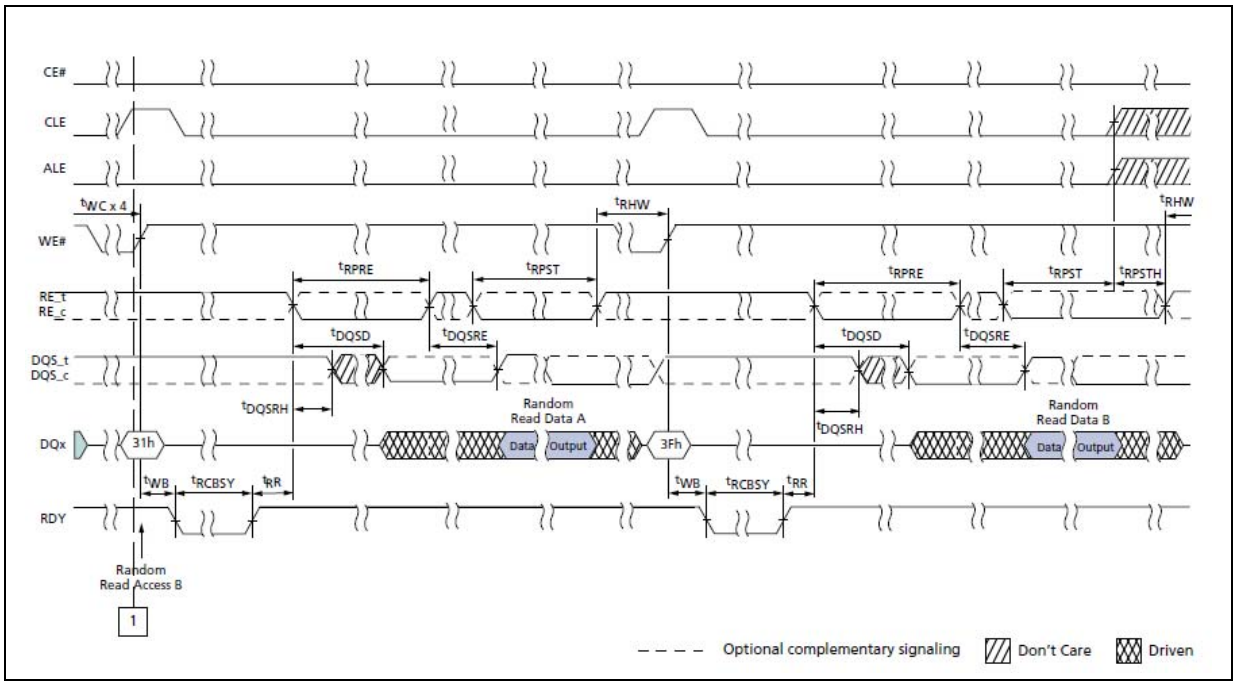


Figure 137. Multi-Plane Read Page (1 of 2)

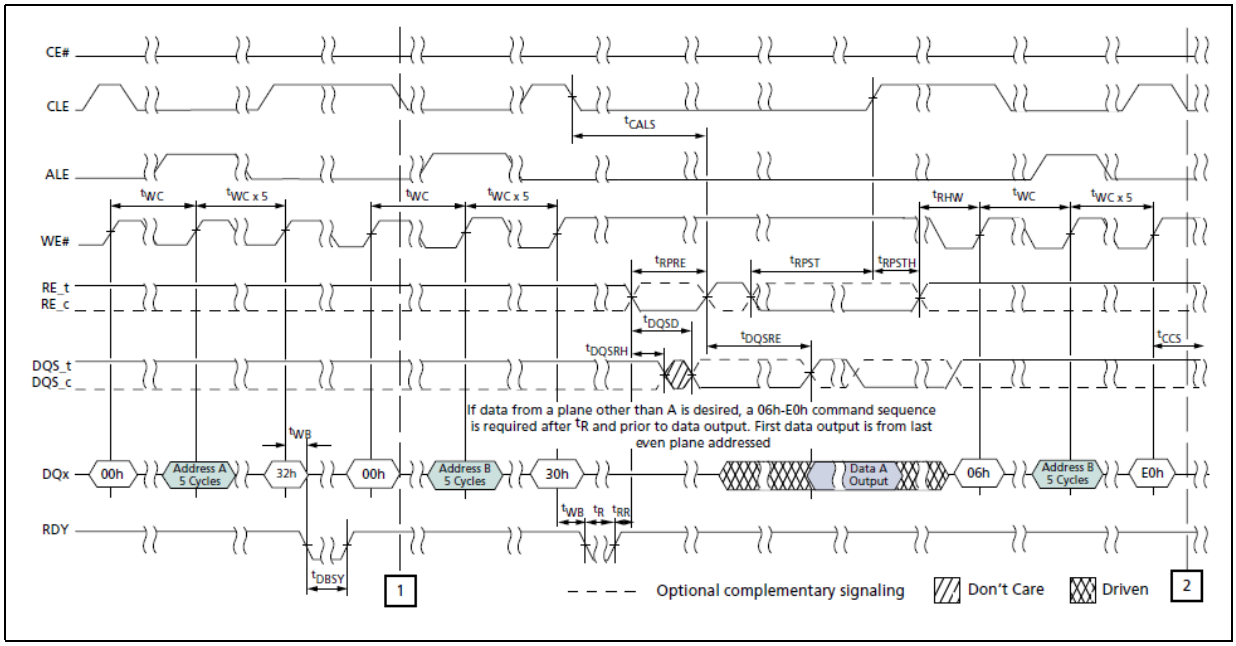


Figure 138. Multi-Plane Read Page (2 of 2)

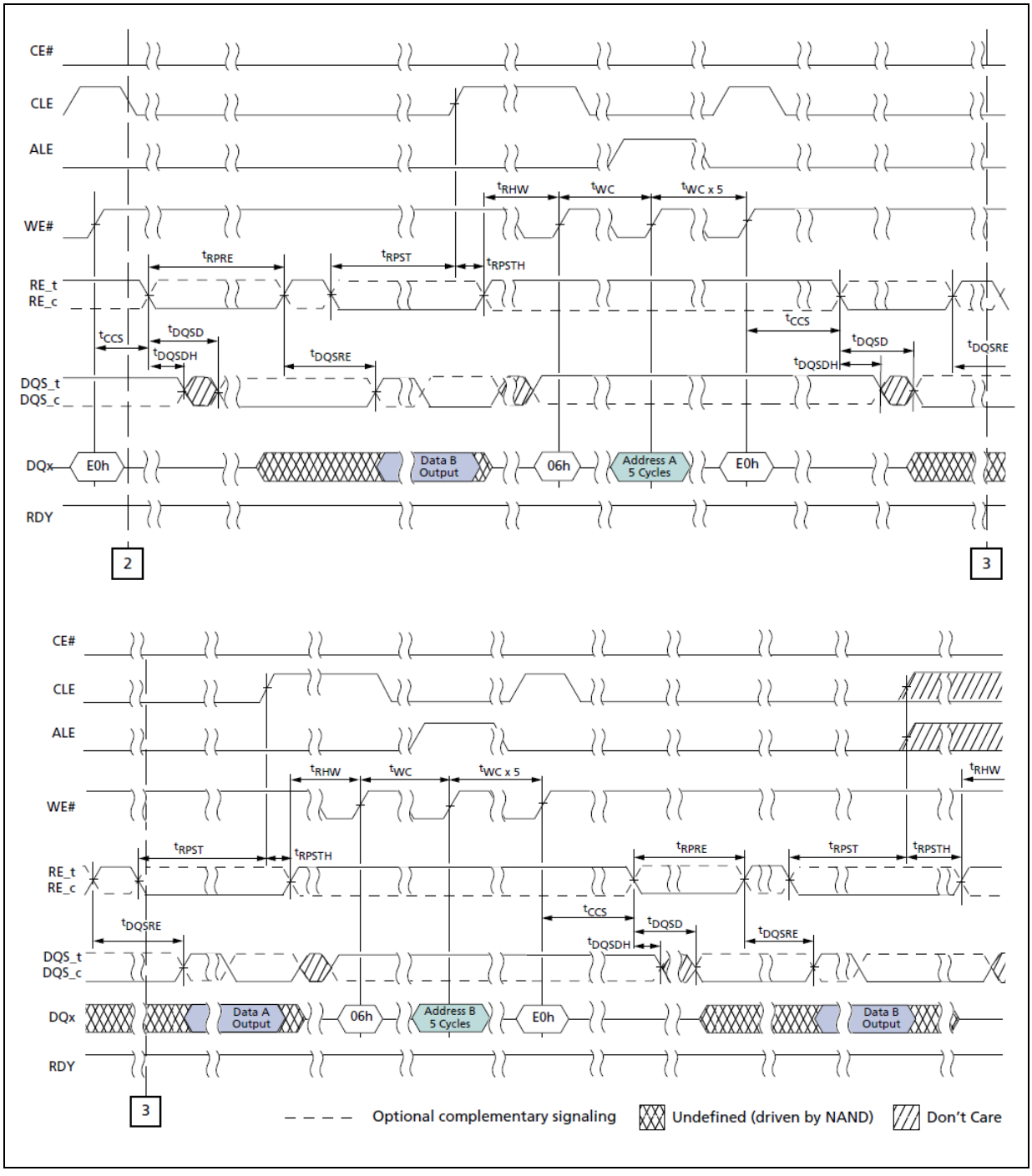


Figure 139. PROGRAM PAGE Operation (1 of 2)

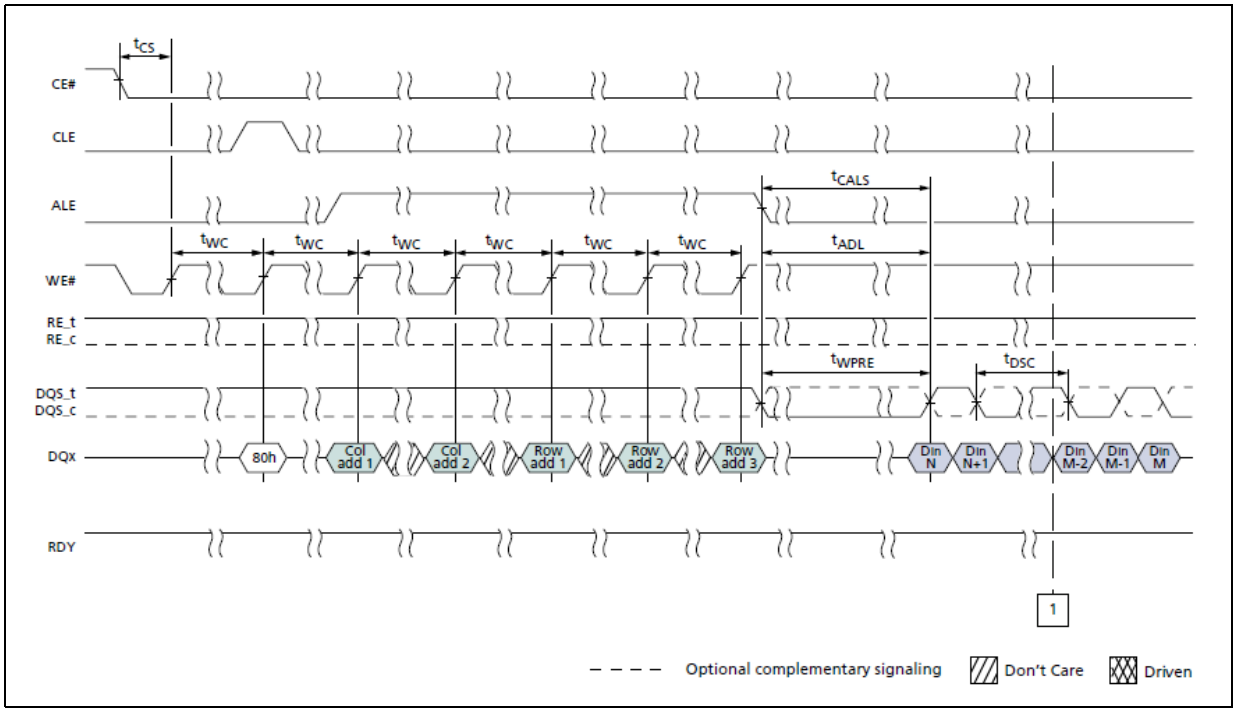


Figure 140. PROGRAM PAGE Operation (2 of 2)

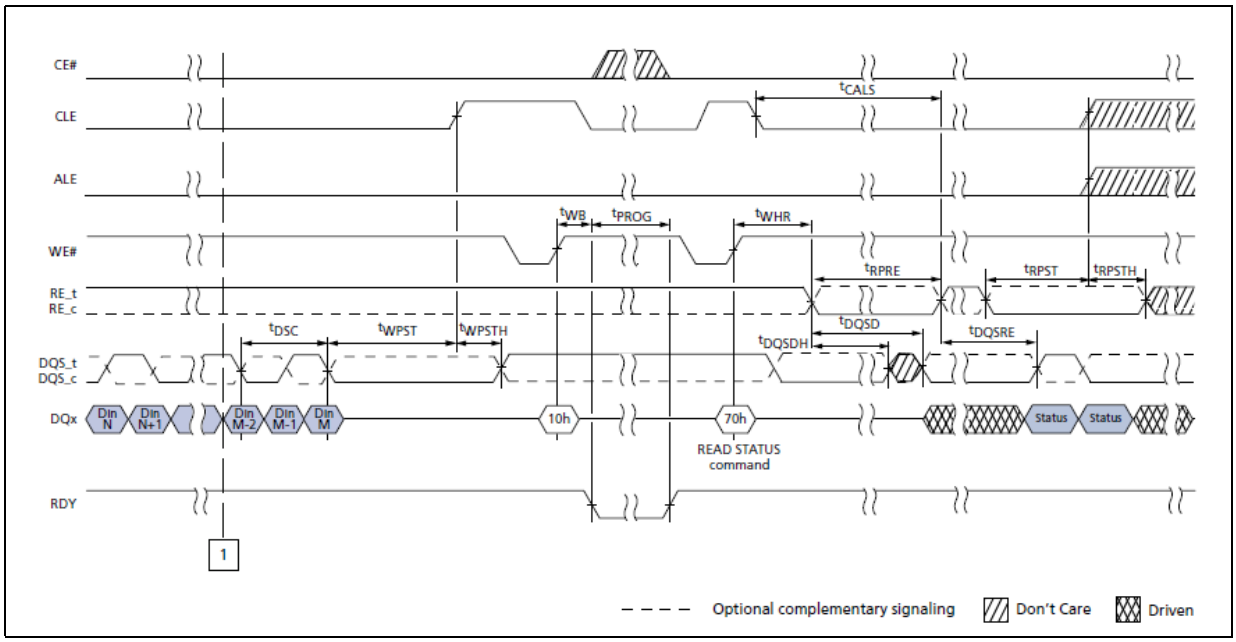


Figure 141. CHANGE WRITE COLUMN

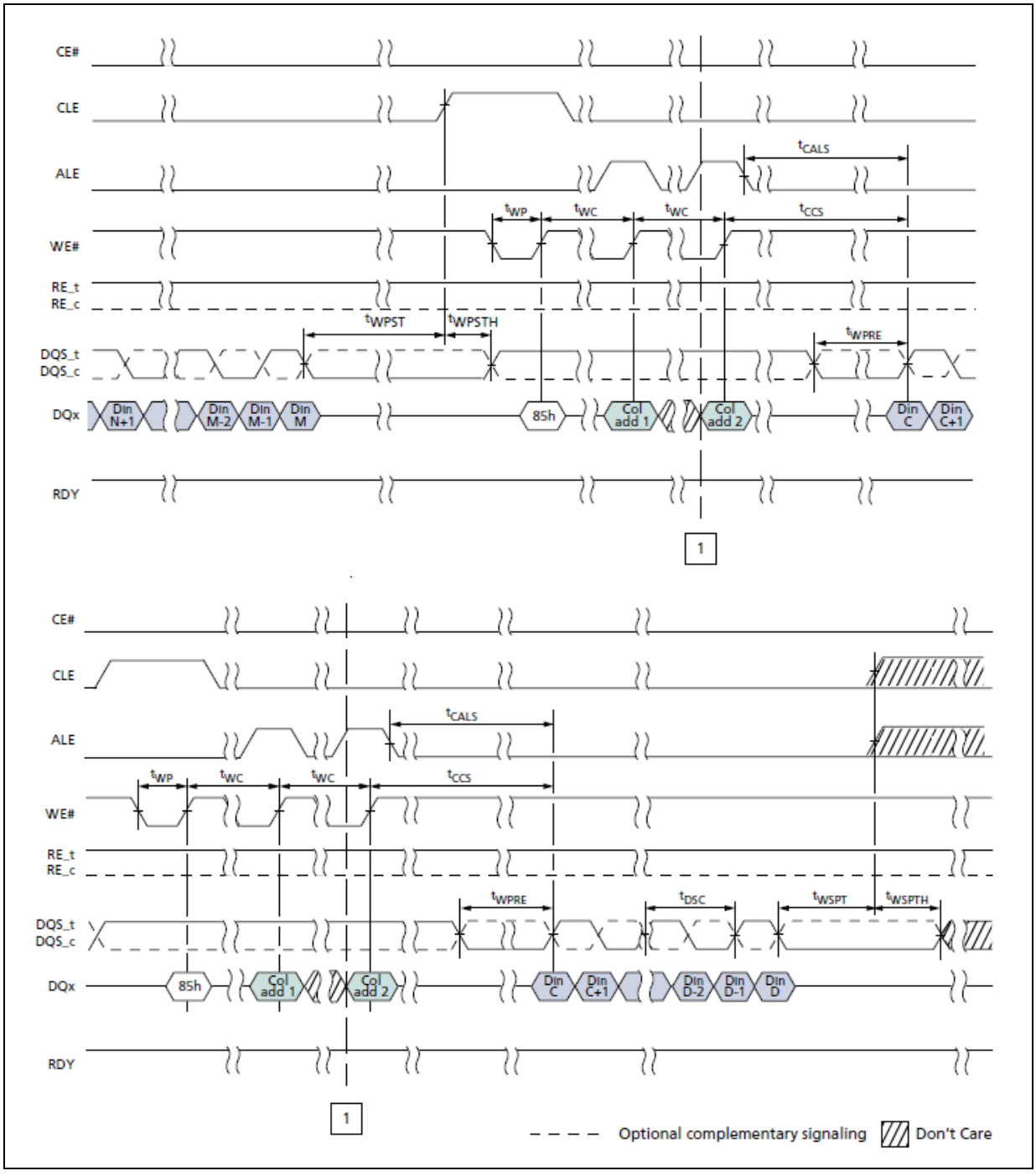


Figure 142. Multi-Plane Program Page

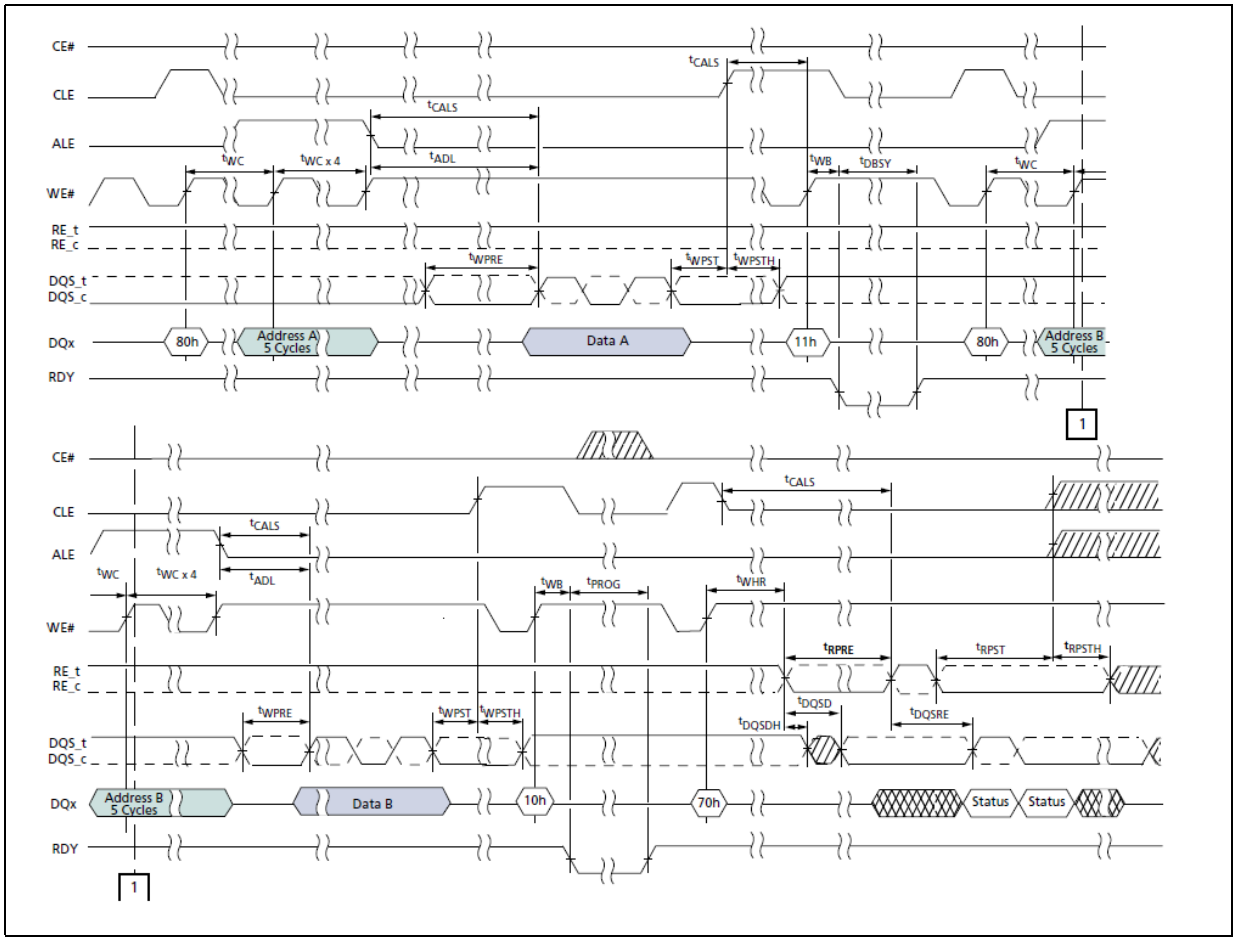


Figure 143. ERASE BLOCK

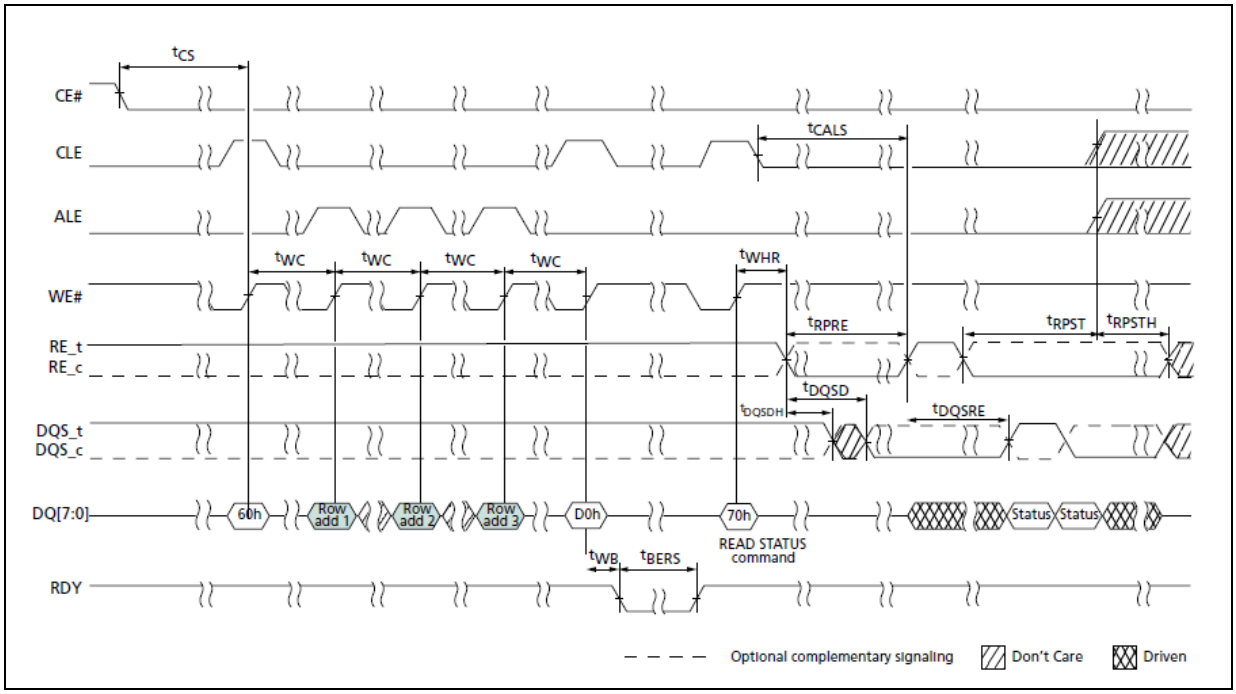


Figure 144. COPYBACK (1 of 3)

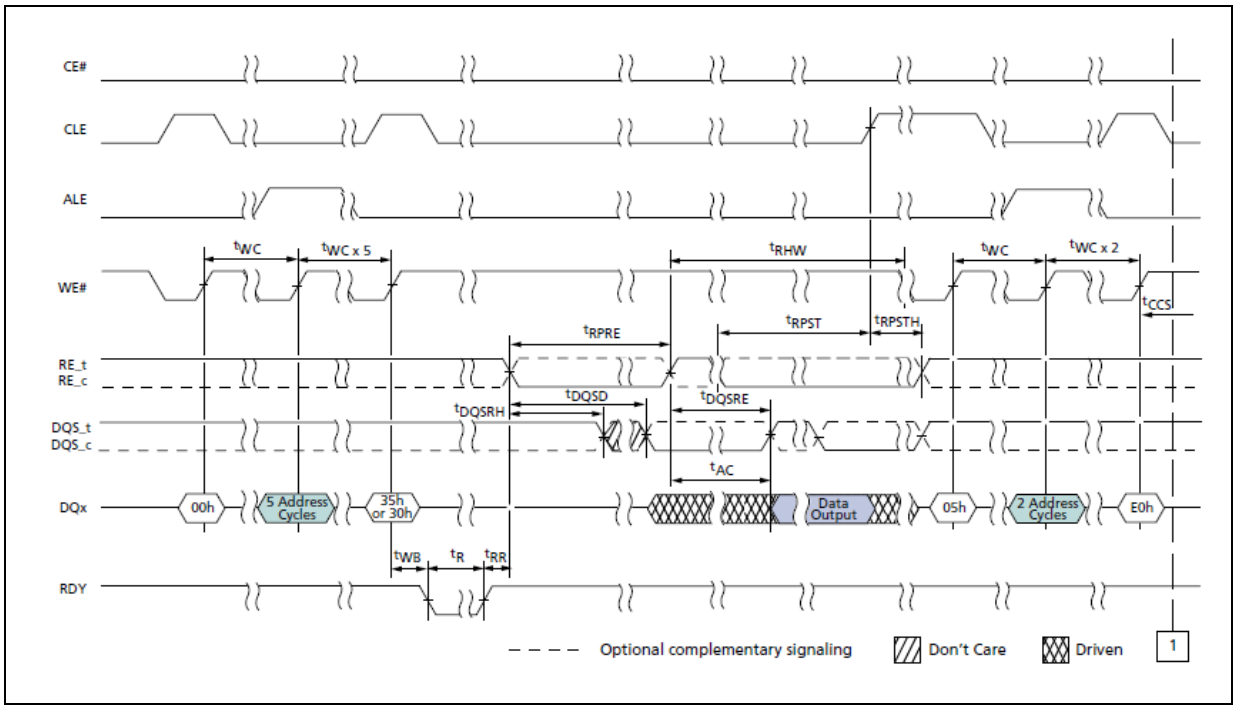


Figure 145. COPYBACK (2 of 3)

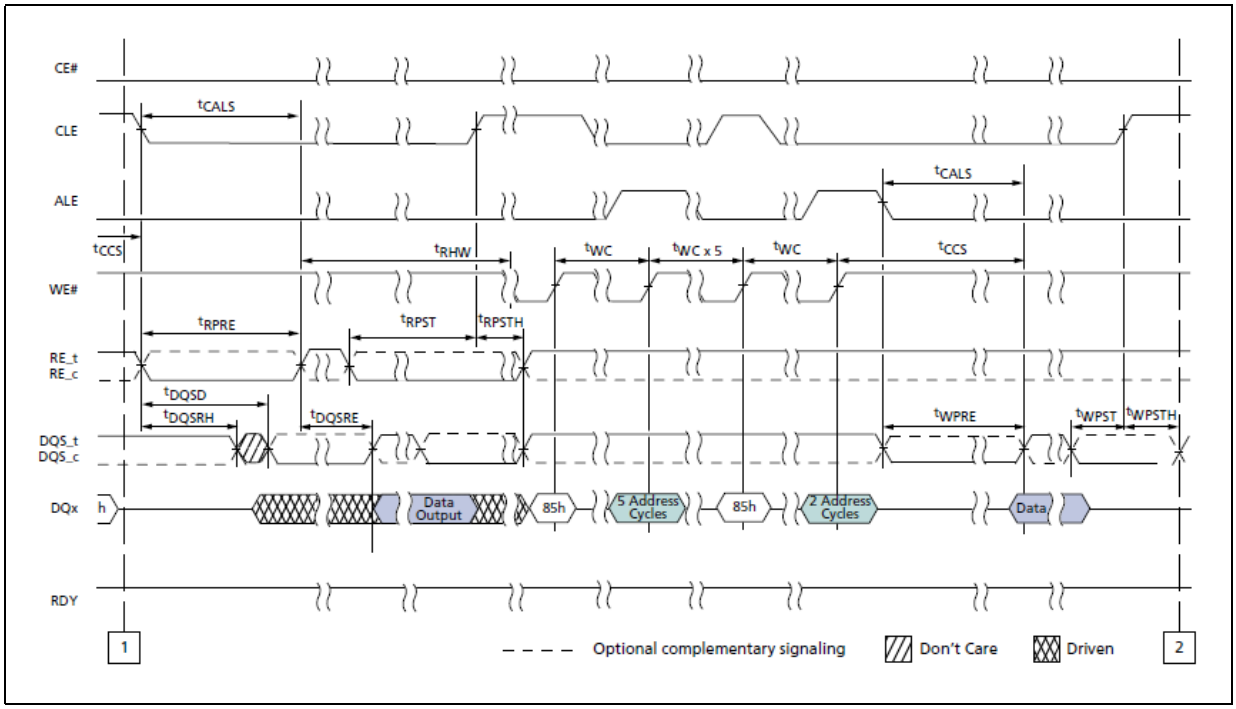
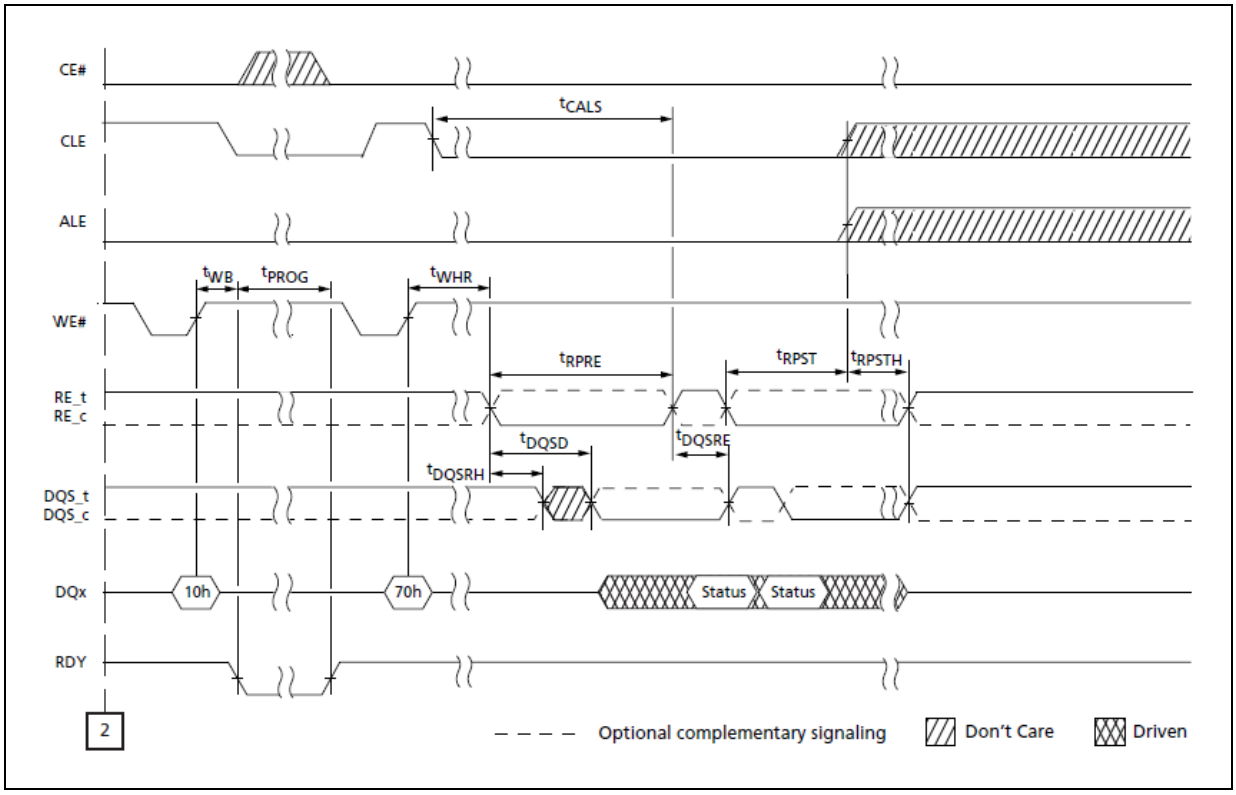


Figure 146. COPYBACK (3 of 3)



37.0 Feature Address 94h: R/B# Configuration

To have more varied usability of the R/B# signal the configuration settings permit use of the R/B# signal in two modes of operation.

The first mode of operation configures the R/B# signal to be LOW during all busy times associated with the NAND device. This is the same R/B# functionality that has been present in all NAND devices prior to the 80-series NAND designs.

The second mode of operation configures the R/B# signal to pulse LOW only after the completion of any busy time associated with the NAND device (tBERS, tCBSY, tDBSY, tFEAT, tITC, tRCBSY, tLPROG, tOBSY, tR, tPROG). The R/B# signal stays HIGH until the completion of the NAND operation which will then pulse LOW for tRBINT.

Table 68. R/B# Feature Factory Trim

Trim	Value
R/B# Pulse feature is not enabled (default)	0
R/B# Pulse feature is enabled	1

Table 69. Feature Address 94h: R/B# Configuration

Sub-Feature Parameter	Options	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	Value
P1										
R/B# signal configuration	R/B# stays LOW during operations (default)								0	0b
	R/B# pulses LOW at completion of operations								1	1b
	Reserved	-	-	-	-	-	-			0b
P2										
Reserved		0	0	0	0	0	0	0	0	00h
P3										
Reserved		0	0	0	0	0	0	0	0	00h
P4										
Reserved		0	0	0	0	0	0	0	0	00h

Table 70. R/B# Timing Parameter when configured for Pulse Operation

Parameter				Value
R/B# LOW time when configured to pulse LOW at the completion of a NAND operation involving R/B#	^{t}RBINT	100	1000	ns

Figure 147. Example of R/B# operation in LOW Operation configuration

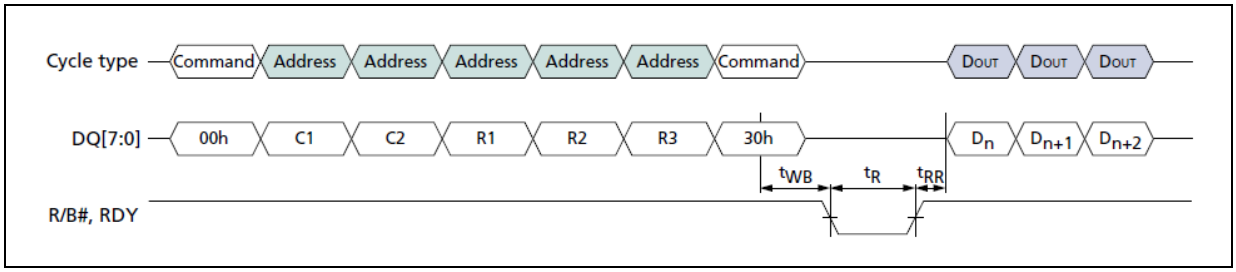
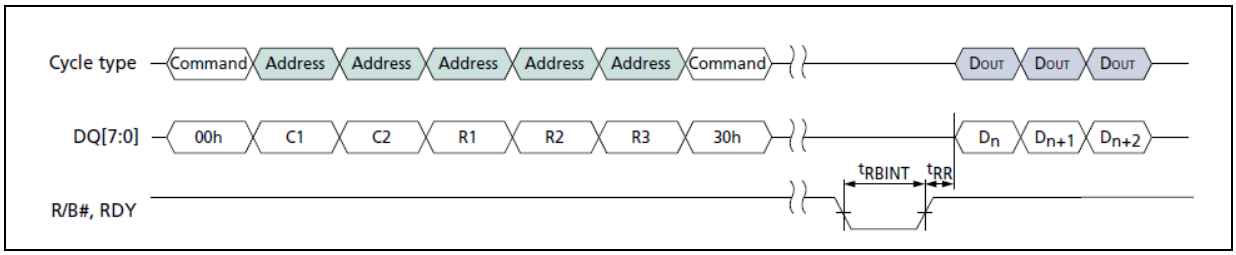


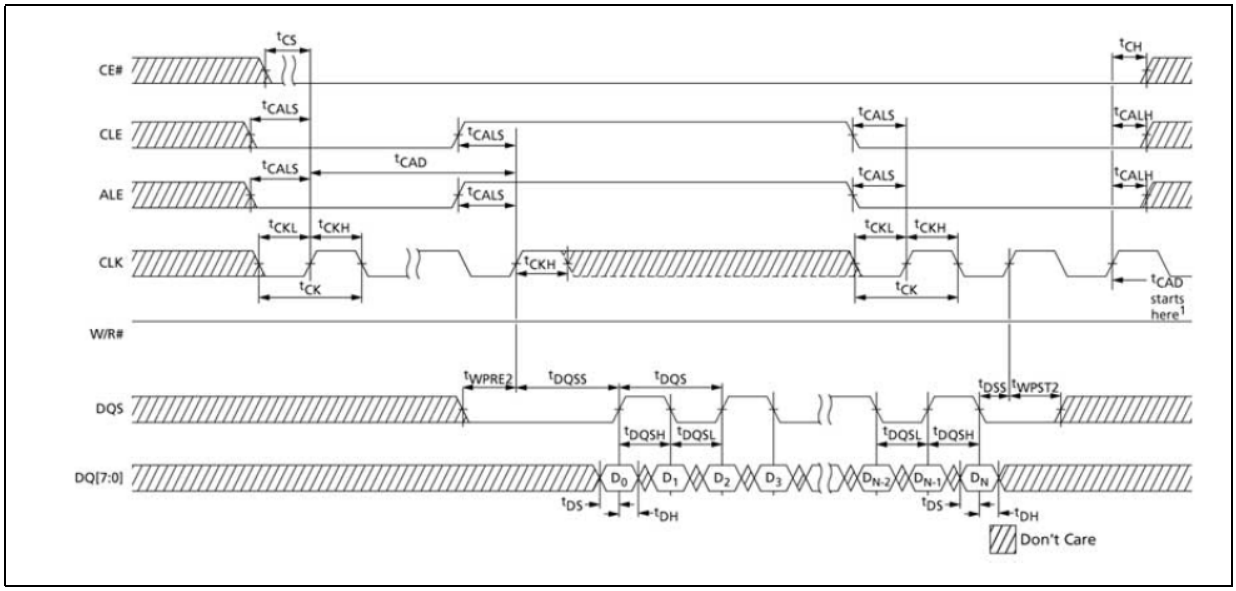
Figure 148. Example of R/B# operation in Pulse Operation configuration



38.0 Synchronous Clock Stop during Data Input

The synchronous data input cycles should accept CLK stopping and starting during data input.

Figure 149. Synchronous Data Input with CLK as "Don't Care"



Notes:
1. ^{t}DQS (AVG) = 5ns and includes jitter spec identical for CLK.
2. ^{t}DQSS (MIN) = 0.75 * tCK; tDQSS (MAX) is undefined.
3. ^{t}WPST2 (MIN) = 0.5 * tCK; tWPST2 (MAX) is undefined.
4. ^{t}WPRE2 (MIN) = 0.5*tCK; tWPRE2 (MAX) in undefined.
5. ^{t}DSS (MIN) = 0.2 * tCK; tDSS (MAX) is undefined.

39.0 References

Use Table 71 to identify standards information referenced in this document.

Table 71. Standards References

Date or Revision Number	Title	Location
February 2008	Open NAND Flash Interface Specification (ONFI) 2.2	http://onfi.org/specifications
March 2011	Open NAND Flash Interface Specification (ONFI) 3.0	http://onfi.org/specifications

40.0 Glossary

Use Table 72 to define terms and acronyms used in this document.

Table 72. Terms and Acronyms

Term	Definition
DDP	Dual (2) Die Package
ECC	Error Correction Code
EDO	Extended Data Output
Gb	Gigabit
GB	Gigabyte In reference to the capacity of this Intel device, the total usable capacity may be less than the total physical capacity because of a small area reserved for NAND flash management and maintenance purposes.
LUN	Logical Unit
MB	Megabyte
ONFI	Open NAND Flash Interface
QDP	Quad (4) Die Package
SDP	Single (1) Die Package
Target	An independent NAND flash component with its own CE# signal
TSOP	Thin Small-Outline Package

41.0 Revision History

Table 73. Document Revision History

Date	Revision	
May 2013	001	Initial release.